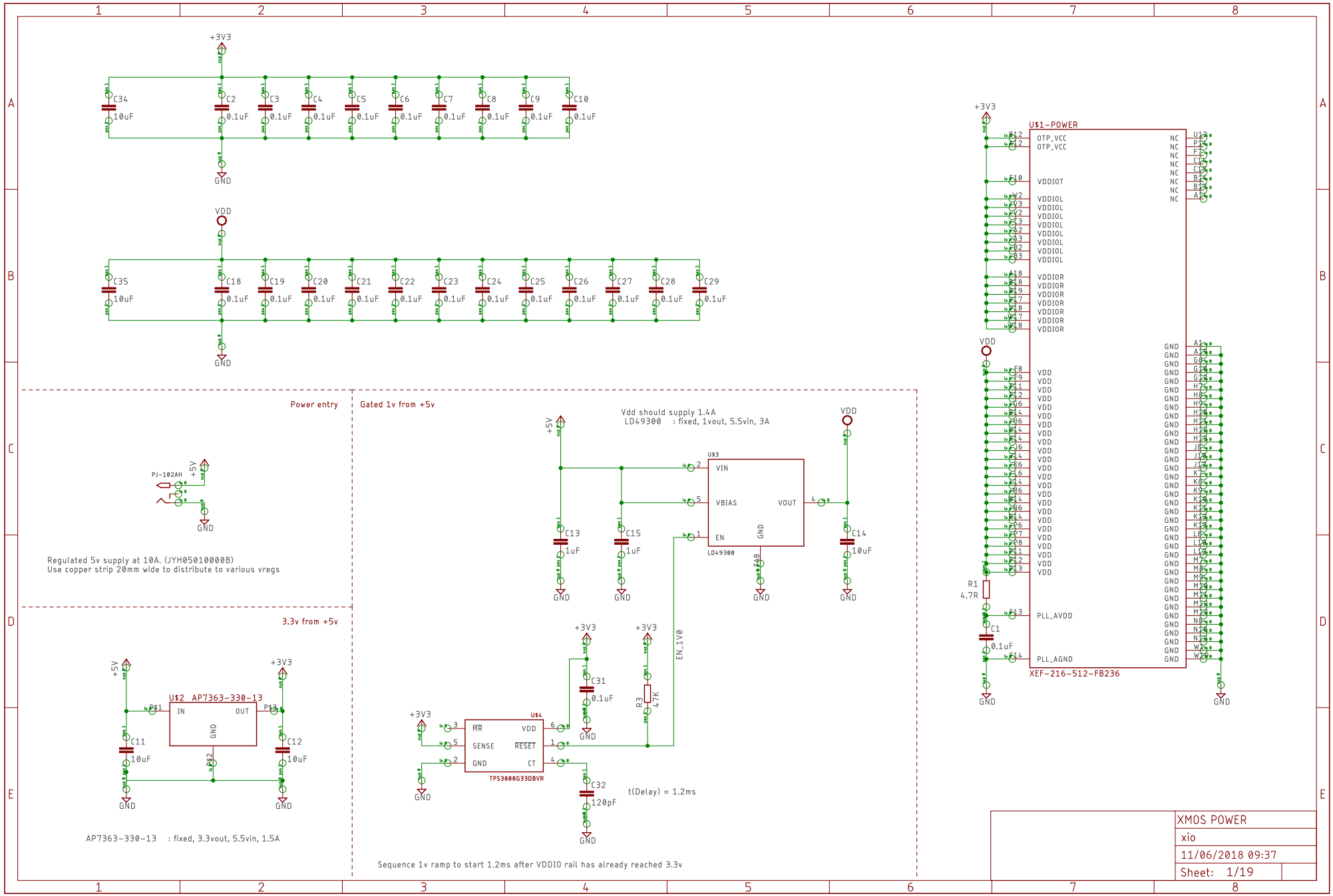
+3V3
C34
10uF
C2
C3
C4
C5
C6
C7
C8
C9
C10
0.1uF
GND
VDD
C35
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
Power entry
PJ-102AH
Regulated 5v supply at 10A. (JYH05010000B)
Use copper strip 20mm wide to distribute to various vregs
Gated 1v from +5v
Vdd should supply 1.4A
LD49300 : fixed, 1vout, 5.5vin, 3A
U$3
VIN
VBIAS
VOUT
EN
LD49300
C13
1uF
C15
C14
10uF
3.3v from +5v
U$2 AP7363-330-13
IN
OUT
C11
C12
AP7363-330-13 : fixed, 3.3vout, 5.5vin, 1.5A
U$4
MR
VDD
SENSE
RESET
CT
TPS3808G33DBVR
C31
0.1uF
R3
47K
EN_1V0
C32
120pF
t(Delay) = 1.2ms
Sequence 1v ramp to start 1.2ms after VDDIO rail has already reached 3.3v
U$1-POWER
OTP_VCC
VDDIOT
VDDIOL
VDDIOR
VDD
PLL_AVDD
PLL_AGND
GND
NC
R1
4.7R
C1
0.1uF
XEF-216-512-FB236
XMOS POWER
xio
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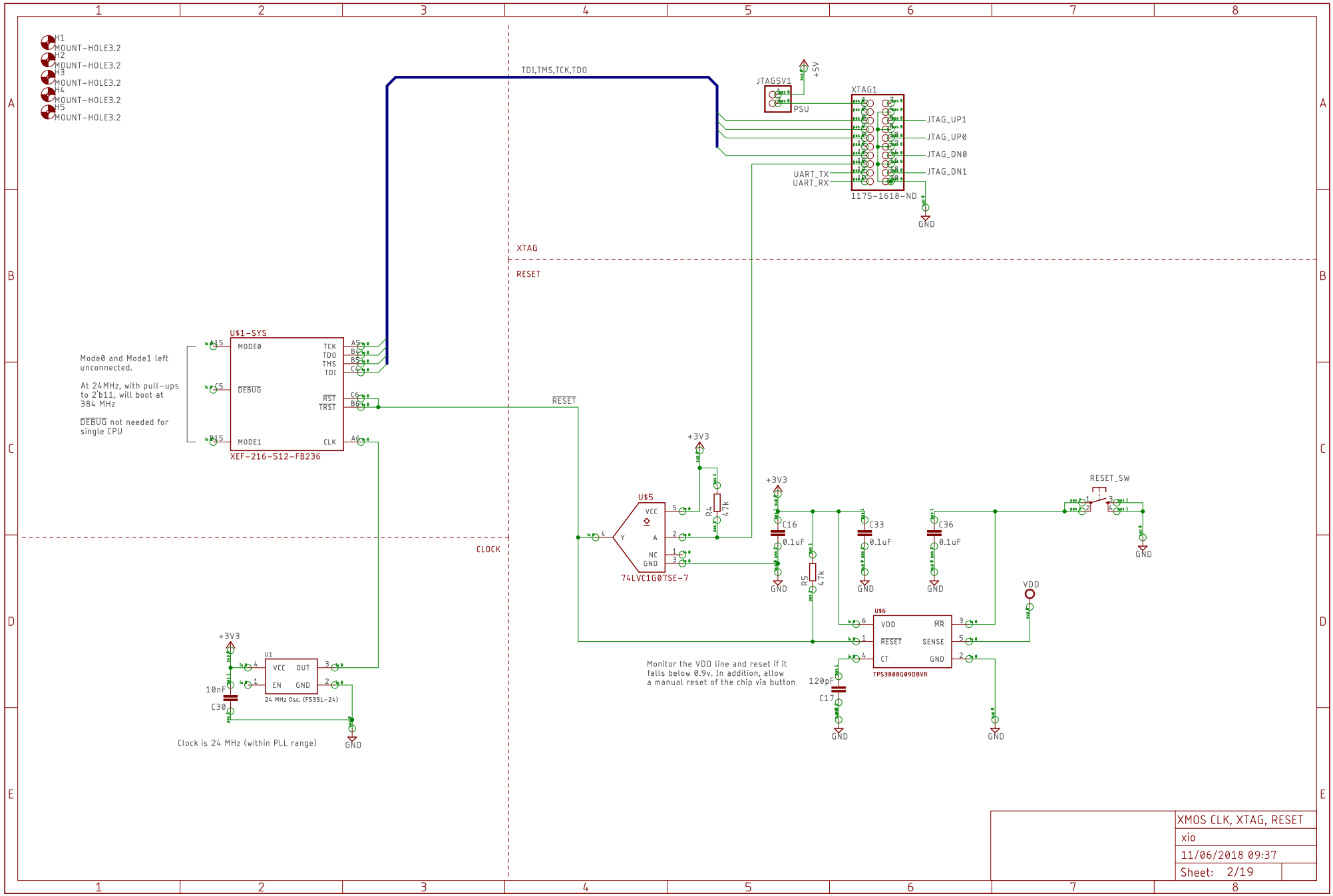
Sheet: 1/19


H1
MOUNT-HOLE3.2
H2
MOUNT-HOLE3.2
H3
MOUNT-HOLE3.2
H4
MOUNT-HOLE3.2
H5
MOUNT-HOLE3.2
TDI,TMS,TCK,TDO
JTAG5V1
+5V
PSU
XTAG1
JTAG_UP1
JTAG_UP0
JTAG_DN0
JTAG_DN1
UART_TX
UART_RX
1175-1618-ND
GND
XTAG
RESET
U$1-SYS
Mode0 and Mode1 left unconnected.
At 24MHz, with pull-ups to 2'b11, will boot at 384 MHz
DEBUG not needed for single CPU
MODE0
DEBUG
MODE1
TCK
TDO
TMS
TDI
RST
TRST
CLK
XEF-216-512-FB236
RESET
+3V3
U$5
VCC
A
NC
GND
74LVC1G07SE-7
R4
4.7k
C16
0.1uF
C33
0.1uF
C36
0.1uF
R5
4.7k
RESET_SW
U$6
VDD
MR
RESET
SENSE
CT
GND
TPS3808G09DBVR
120pF
C17
Monitor the VDD line and reset if it falls below 0.9v. In addition, allow a manual reset of the chip via button
CLOCK
U1
VCC
OUT
EN
GND
24 MHz Osc. (F535L-24)
10nF
C30
Clock is 24 MHz (within PLL range)
XMOS CLK, XTAG, RESET
xio
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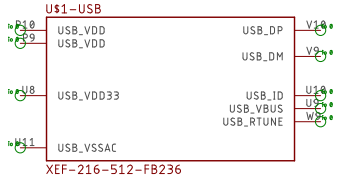
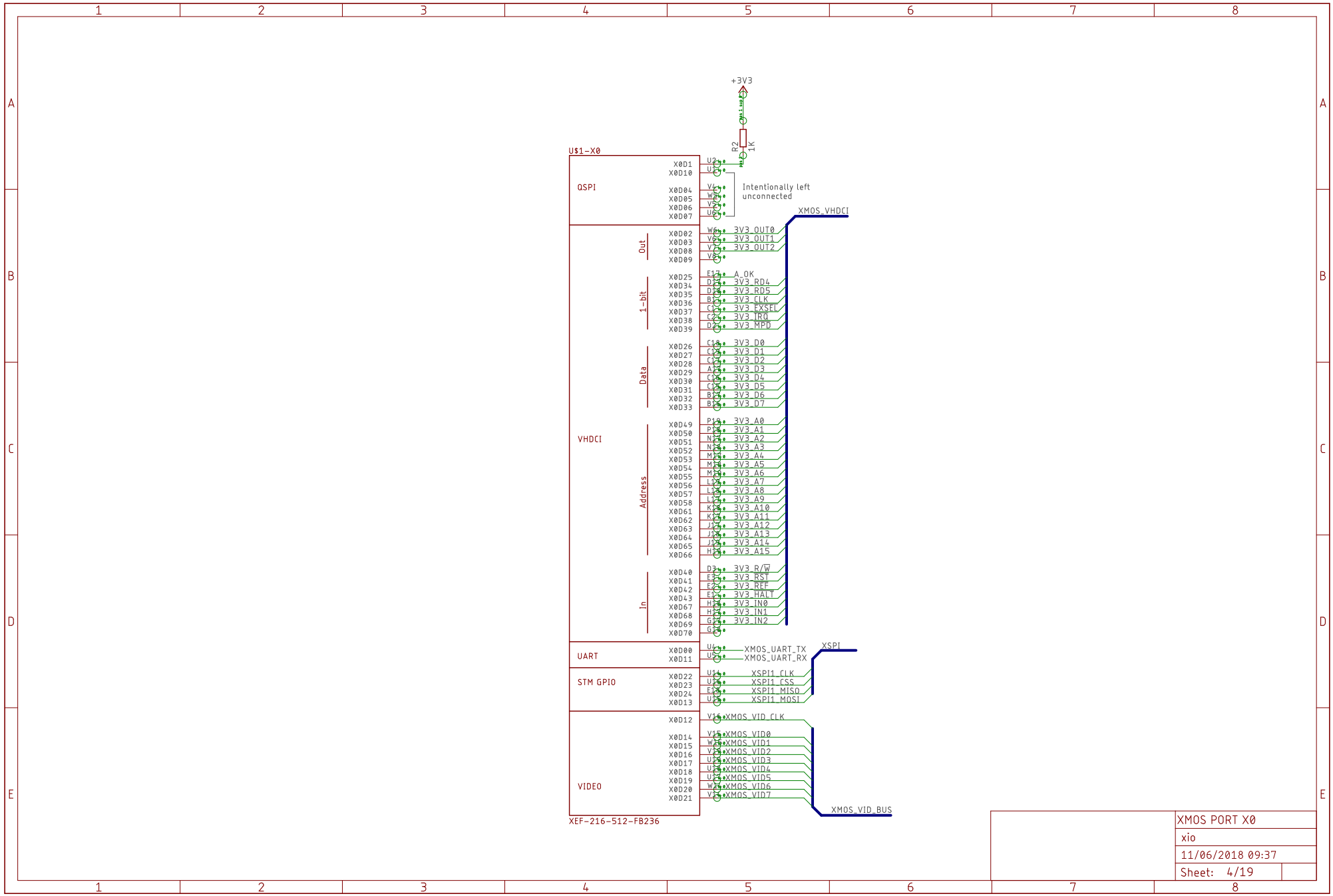
Sheet: 2/19

USB not used in this design



	XMOS USB
	xio
	11/06/2018 09:37
	Sheet: 3/19


+3V3
R2
1K
U$1-X0
QSPI
VHDCI
Out
1-bit
Data
Address
In
UART
STM GPIO
VIDEO
XEF-216-512-FB236
Intentionally left unconnected
XMOS_VHDCI
3V3_OUT0
3V3_OUT1
3V3_OUT2
A_OK
3V3_RD4
3V3_RD5
3V3_CLK
3V3_EXSEL
3V3_IRQ
3V3_MPD
3V3_D0
3V3_D1
3V3_D2
3V3_D3
3V3_D4
3V3_D5
3V3_D6
3V3_D7
3V3_A0
3V3_A1
3V3_A2
3V3_A3
3V3_A4
3V3_A5
3V3_A6
3V3_A7
3V3_A8
3V3_A9
3V3_A10
3V3_A11
3V3_A12
3V3_A13
3V3_A14
3V3_A15
3V3_R/W
3V3_RST
3V3_REF
3V3_HALT
3V3_IN0
3V3_IN1
3V3_IN2
XMOS_UART_TX
XMOS_UART_RX
XSPI
XSPI1_CLK
XSPI1_CSS
XSPI1_MISO
XSPI1_MOSI
XMOS_VID_CLK
XMOS_VID0
XMOS_VID1
XMOS_VID2
XMOS_VID3
XMOS_VID4
XMOS_VID5
XMOS_VID6
XMOS_VID7
XMOS_VID_BUS
XMOS PORT X0
xio
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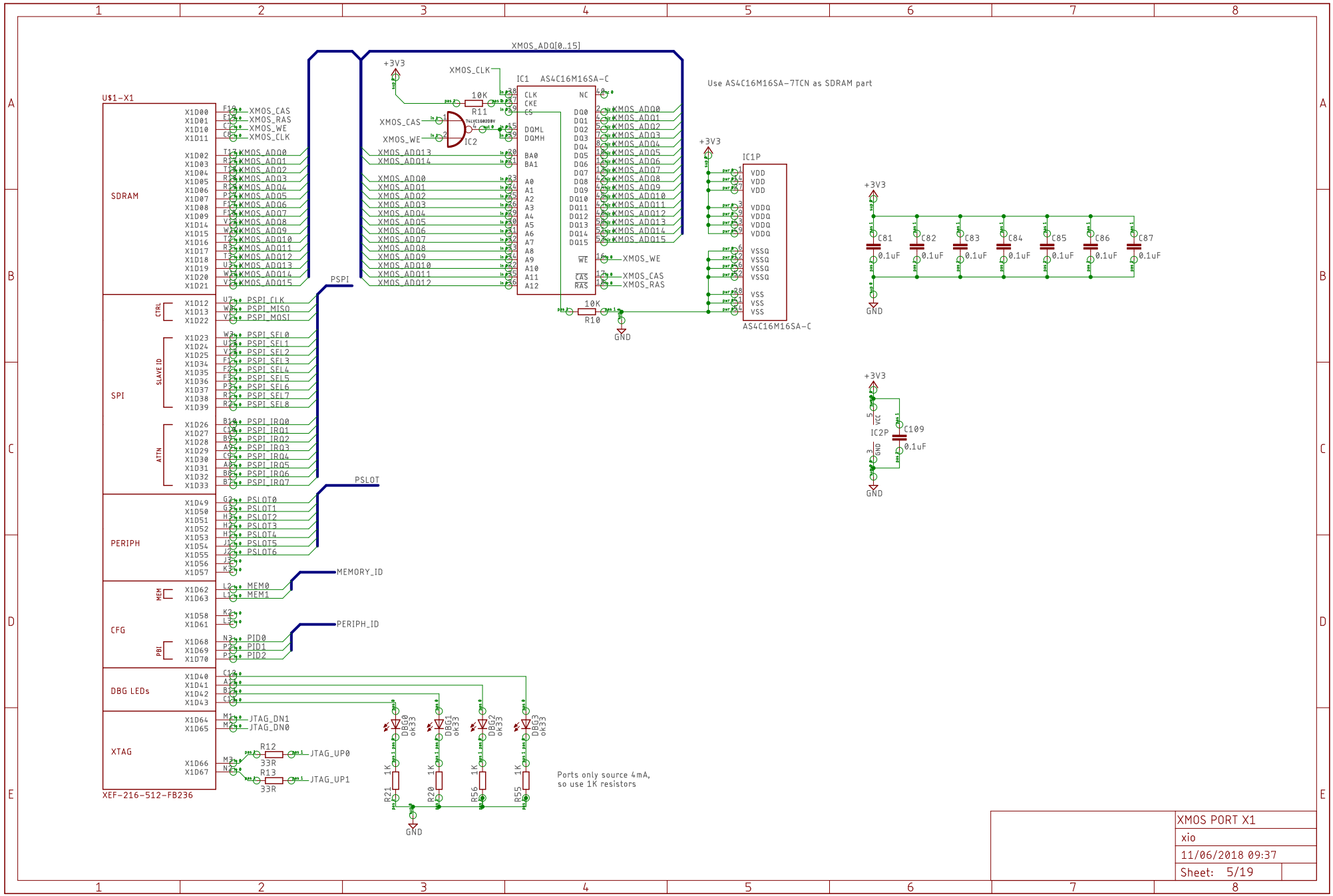
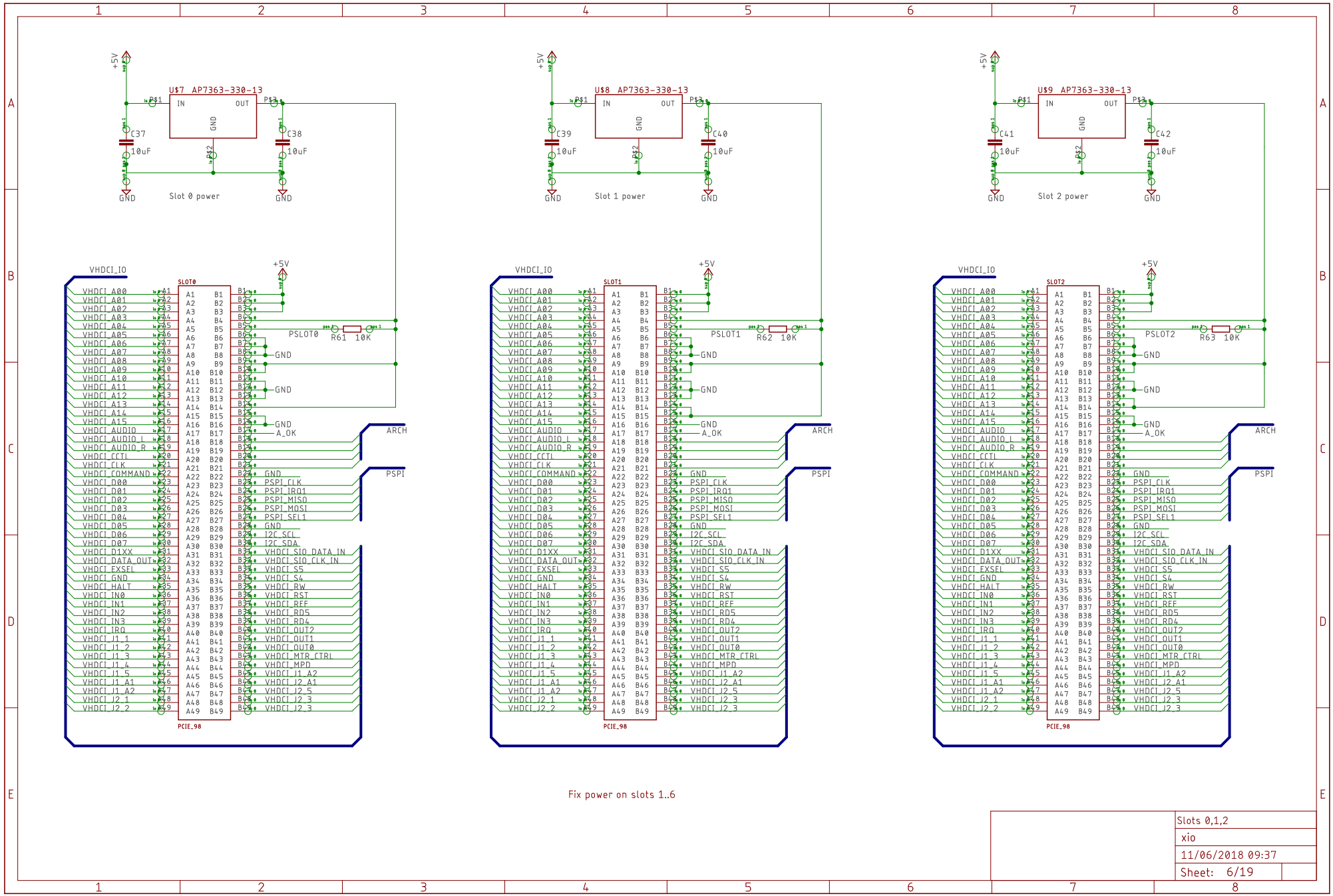
Sheet: 4/19


XMOS_ADQ[0..15]
U$1-X1
SDRAM
SPI
PERIPH
CFG
DBG LEDs
XTAG
XEF-216-512-FB236
PSPI
PSLOT
MEMORY_ID
PERIPH_ID
IC1 AS4C16M16SA-C
Use AS4C16M16SA-7TCN as SDRAM part
IC1P
AS4C16M16SA-C
IC2P
Ports only source 4mA, so use 1K resistors
XMOS PORT X1
xio
11/06/2018 09:37
Sheet: 5/19


U$7 AP7363-330-13
U$8 AP7363-330-13
U$9 AP7363-330-13
IN
OUT
GND
+5V
C37 10uF
C38 10uF
C39 10uF
C40 10uF
C41 10uF
C42 10uF
Slot 0 power
Slot 1 power
Slot 2 power
VHDCI_IO
SLOT0
SLOT1
SLOT2
PCIE_98
PSLOT0
PSLOT1
PSLOT2
R61 10K
R62 10K
R63 10K
ARCH
PSPI
A_OK
PSPI_CLK
PSPI_IRQ1
PSPI_MISO
PSPI_MOSI
PSPI_SEL1
I2C_SCL
I2C_SDA
VHDCI_SIO_DATA_IN
VHDCI_SIO_CLK_IN
VHDCI_S5
VHDCI_S4
VHDCI_RW
VHDCI_RST
VHDCI_REF
VHDCI_RD5
VHDCI_RD4
VHDCI_OUT2
VHDCI_OUT1
VHDCI_OUT0
VHDCI_MTR_CTRL
VHDCI_MPD
VHDCI_J1_A2
VHDCI_J2_A1
VHDCI_J2_5
VHDCI_J2_3
Fix power on slots 1..6
Slots 0,1,2
xio
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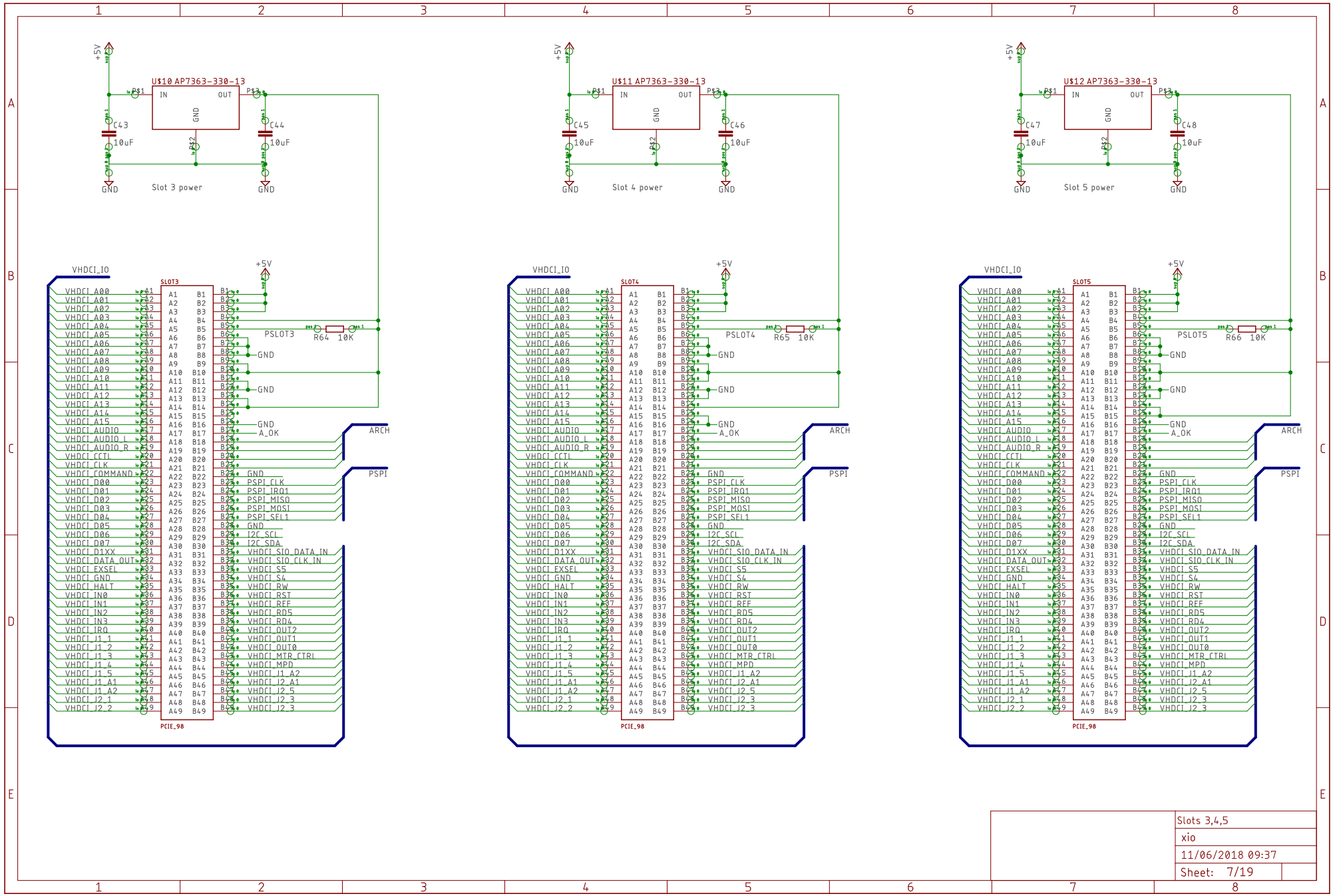
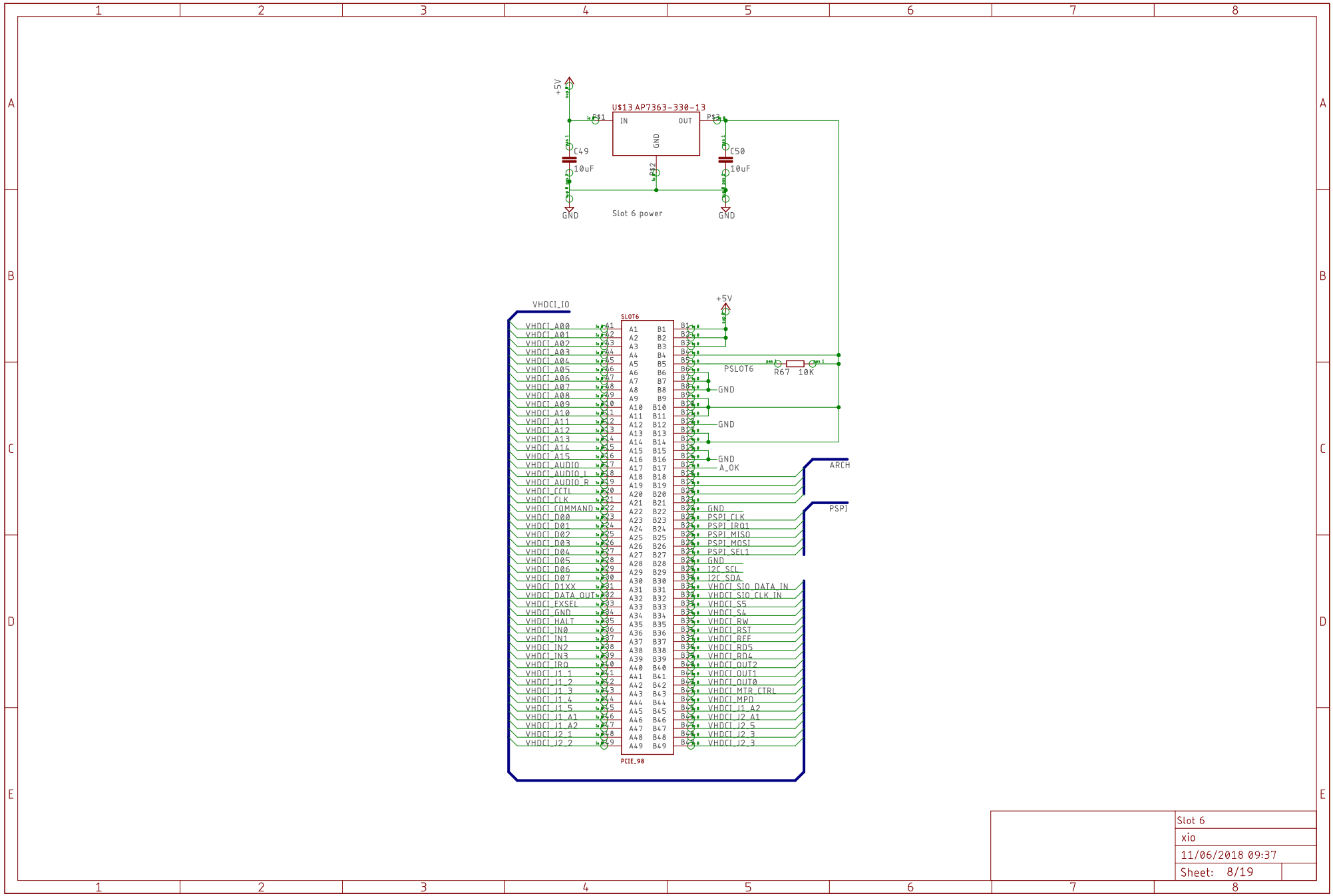

U$10 AP7363-330-13
U$11 AP7363-330-13
U$12 AP7363-330-13
IN
OUT
GND
C43 10uF
C44 10uF
C45 10uF
C46 10uF
C47 10uF
C48 10uF
Slot 3 power
Slot 4 power
Slot 5 power
+5V
VHDCI_IO
SLOT3
SLOT4
SLOT5
PCIE_98
PSLOT3
PSLOT4
PSLOT5
R64 10K
R65 10K
R66 10K
ARCH
PSPI
A_OK
PSPI_CLK
PSPI_IRQ1
PSPI_MISO
PSPI_MOSI
PSPI_SEL1
I2C_SCL
I2C_SDA
VHDCI_SIO_DATA_IN
VHDCI_SIO_CLK_IN
Slots 3,4,5
xio
11/06/2018 09:37
Sheet: 7/19



	Slot 6
	xio
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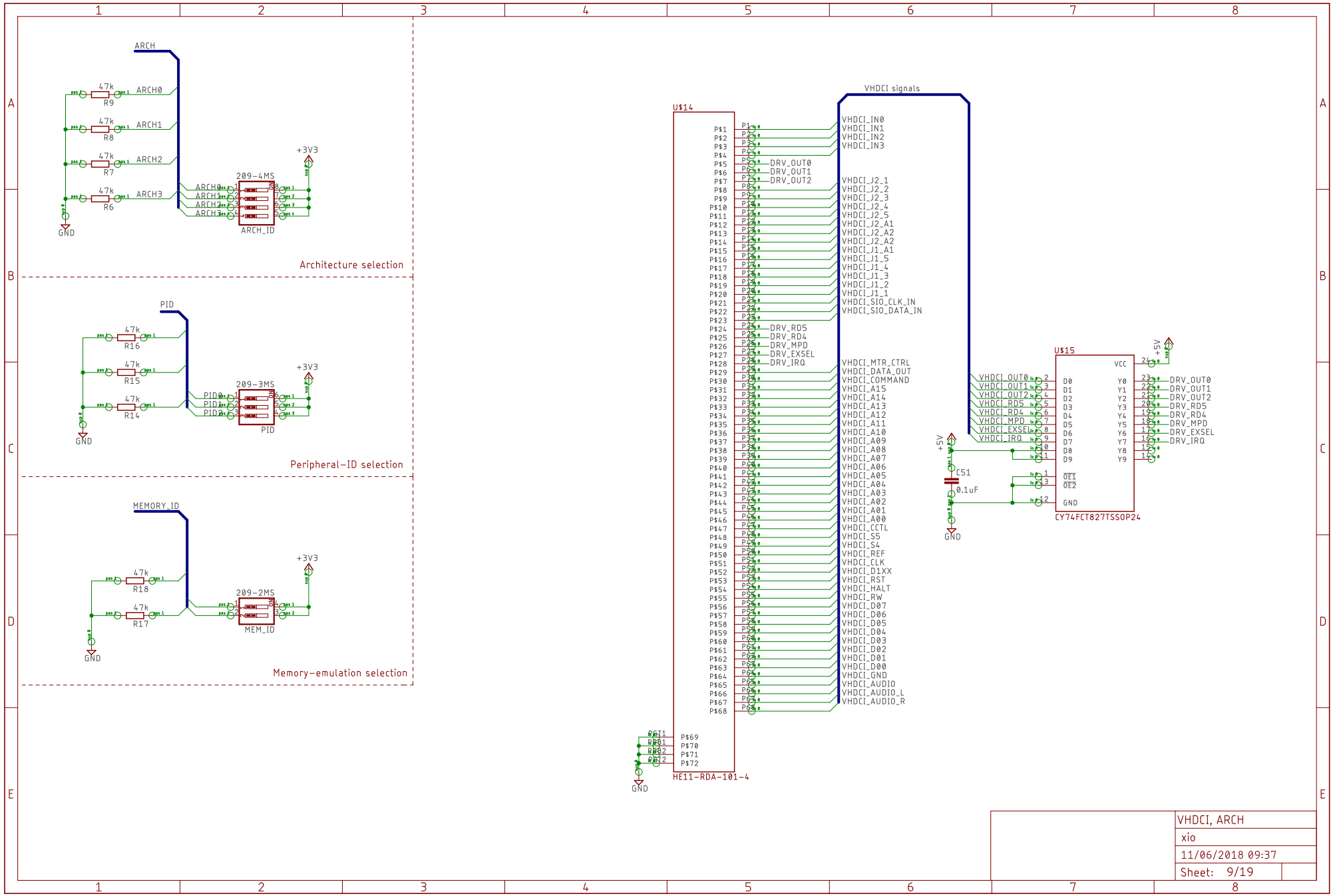
	Sheet: 8/19


ARCH
47k
R9
ARCH0
47k
R8
ARCH1
47k
R7
ARCH2
47k
R6
ARCH3
GND
209-4MS
ARCH0
ARCH1
ARCH2
ARCH3
ARCH_ID
+3V3
Architecture selection
PID
47k
R16
47k
R15
47k
R14
GND
209-3MS
PID0
PID1
PID2
PID
+3V3
Peripheral-ID selection
MEMORY_ID
47k
R18
47k
R17
GND
209-2MS
MEM_ID
+3V3
Memory-emulation selection
VHDCI signals
U$14
P$1
P$2
P$3
P$4
P$5
P$6
P$7
P$8
P$9
P$10
P$11
P$12
P$13
P$14
P$15
P$16
P$17
P$18
P$19
P$20
P$21
P$22
P$23
P$24
P$25
P$26
P$27
P$28
P$29
P$30
P$31
P$32
P$33
P$34
P$35
P$36
P$37
P$38
P$39
P$40
P$41
P$42
P$43
P$44
P$45
P$46
P$47
P$48
P$49
P$50
P$51
P$52
P$53
P$54
P$55
P$56
P$57
P$58
P$59
P$60
P$61
P$62
P$63
P$64
P$65
P$66
P$67
P$68
P$69
P$70
P$71
P$72
VHDCI_IN0
VHDCI_IN1
VHDCI_IN2
VHDCI_IN3
DRV_OUT0
DRV_OUT1
DRV_OUT2
VHDCI_J2_1
VHDCI_J2_2
VHDCI_J2_3
VHDCI_J2_4
VHDCI_J2_5
VHDCI_J2_A1
VHDCI_J2_A2
VHDCI_J2_A2
VHDCI_J1_A1
VHDCI_J1_5
VHDCI_J1_4
VHDCI_J1_3
VHDCI_J1_2
VHDCI_J1_1
VHDCI_SIO_CLK_IN
VHDCI_SIO_DATA_IN
DRV_RD5
DRV_RD4
DRV_MPD
DRV_EXSEL
DRV_IRQ
VHDCI_MTR_CTRL
VHDCI_DATA_OUT
VHDCI_COMMAND
VHDCI_A15
VHDCI_A14
VHDCI_A13
VHDCI_A12
VHDCI_A11
VHDCI_A10
VHDCI_A09
VHDCI_A08
VHDCI_A07
VHDCI_A06
VHDCI_A05
VHDCI_A04
VHDCI_A03
VHDCI_A02
VHDCI_A01
VHDCI_A00
VHDCI_CCTL
VHDCI_S5
VHDCI_S4
VHDCI_REF
VHDCI_CLK
VHDCI_D1XX
VHDCI_RST
VHDCI_HALT
VHDCI_RW
VHDCI_D07
VHDCI_D06
VHDCI_D05
VHDCI_D04
VHDCI_D03
VHDCI_D02
VHDCI_D01
VHDCI_D00
VHDCI_GND
VHDCI_AUDIO
VHDCI_AUDIO_L
VHDCI_AUDIO_R
GND
HE11-RDA-101-4
U$15
VHDCI_OUT0
VHDCI_OUT1
VHDCI_OUT2
VHDCI_RD5
VHDCI_RD4
VHDCI_MPD
VHDCI_EXSEL
VHDCI_IRQ
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
OE1
OE2
GND
VCC
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
DRV_OUT0
DRV_OUT1
DRV_OUT2
DRV_RD5
DRV_RD4
DRV_MPD
DRV_EXSEL
DRV_IRQ
+5V
C51
0.1uF
CY74FCT827TSSOP24
VHDCI, ARCH
xio
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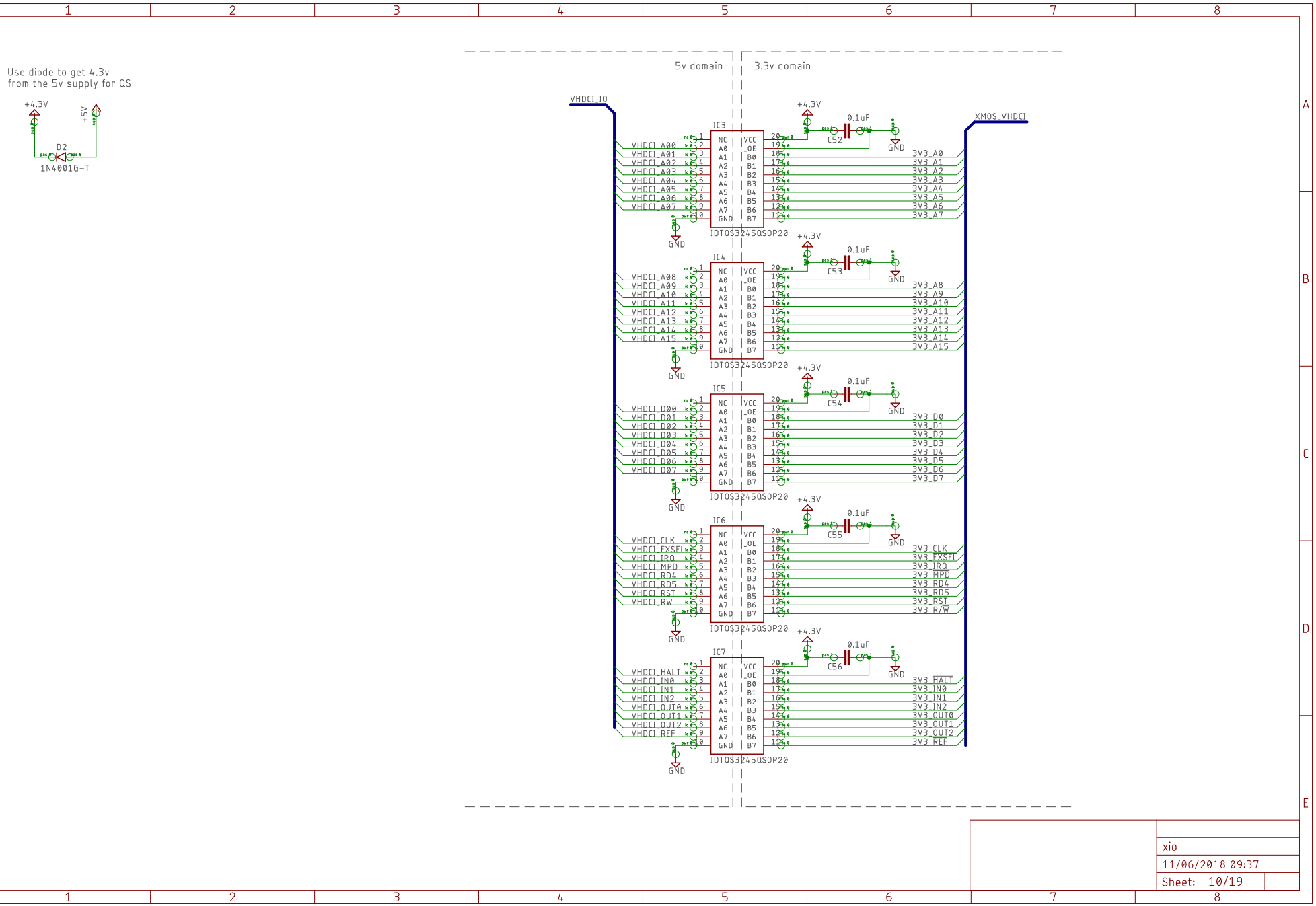
Sheet: 9/19


Use diode to get 4.3v
from the 5v supply for QS
+4.3V
+5V
D2
1N4001G-T
5v domain
3.3v domain
VHDCI_IO
XMOS_VHDCI
IC3
IC4
IC5
IC6
IC7
IDTQS32245QSOP20
+4.3V
0.1uF
C52
C53
C54
C55
C56
GND
VHDCI_A00
VHDCI_A01
VHDCI_A02
VHDCI_A03
VHDCI_A04
VHDCI_A05
VHDCI_A06
VHDCI_A07
3V3_A0
3V3_A1
3V3_A2
3V3_A3
3V3_A4
3V3_A5
3V3_A6
3V3_A7
VHDCI_A08
VHDCI_A09
VHDCI_A10
VHDCI_A11
VHDCI_A12
VHDCI_A13
VHDCI_A14
VHDCI_A15
3V3_A8
3V3_A9
3V3_A10
3V3_A11
3V3_A12
3V3_A13
3V3_A14
3V3_A15
VHDCI_D00
VHDCI_D01
VHDCI_D02
VHDCI_D03
VHDCI_D04
VHDCI_D05
VHDCI_D06
VHDCI_D07
3V3_D0
3V3_D1
3V3_D2
3V3_D3
3V3_D4
3V3_D5
3V3_D6
3V3_D7
VHDCI_CLK
VHDCI_EXSEL
VHDCI_IRQ
VHDCI_MPD
VHDCI_RD4
VHDCI_RD5
VHDCI_RST
VHDCI_RW
3V3_CLK
3V3_EXSEL
3V3_IRQ
3V3_MPD
3V3_RD4
3V3_RD5
3V3_RST
3V3_R/W
VHDCI_HALT
VHDCI_IN0
VHDCI_IN1
VHDCI_IN2
VHDCI_OUT0
VHDCI_OUT1
VHDCI_OUT2
VHDCI_REF
3V3_HALT
3V3_IN0
3V3_IN1
3V3_IN2
3V3_OUT0
3V3_OUT1
3V3_OUT2
3V3_REF
xio
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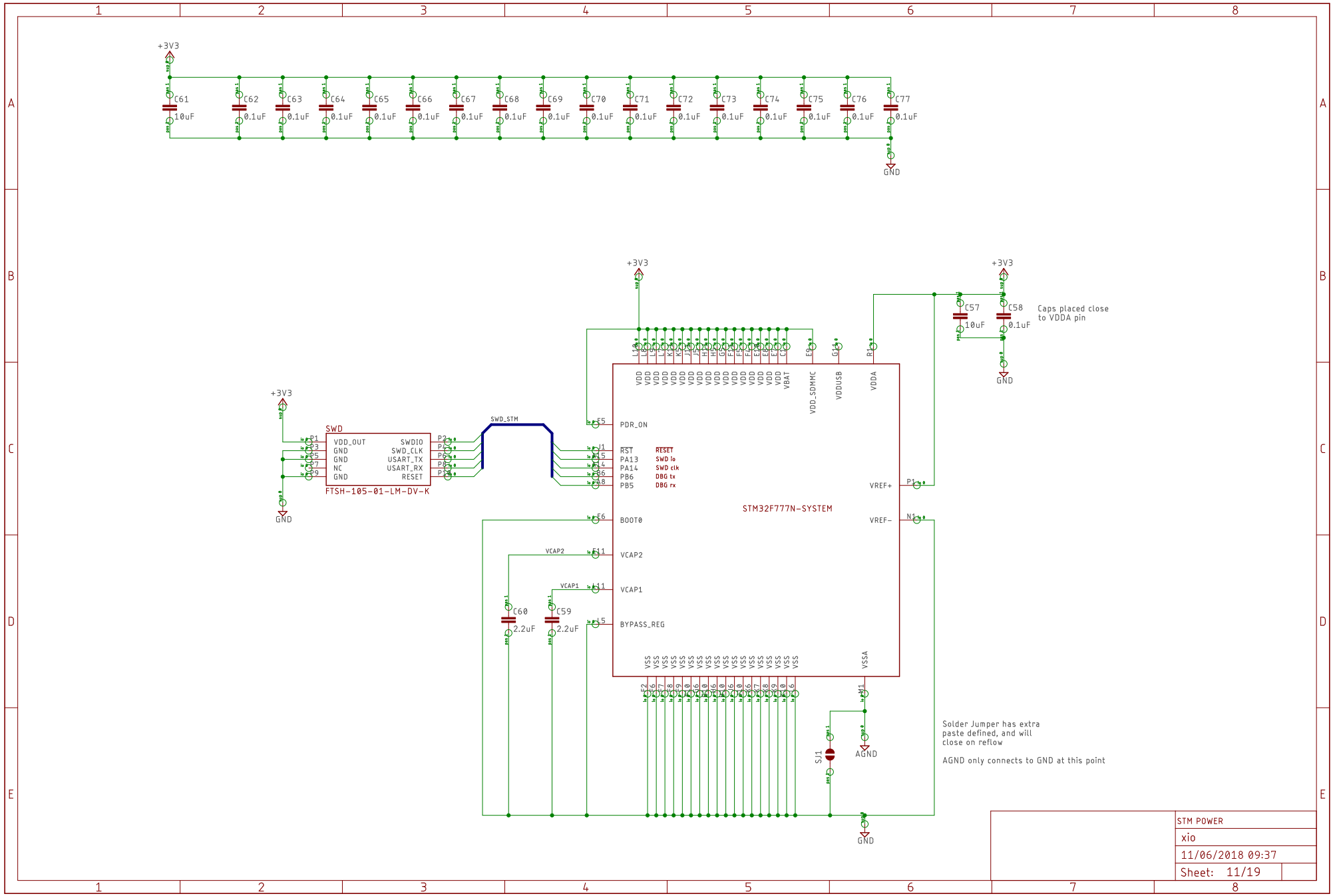
Sheet: 10/19


+3V3
C61
10uF
C62
0.1uF
C63
0.1uF
C64
0.1uF
C65
0.1uF
C66
0.1uF
C67
0.1uF
C68
0.1uF
C69
0.1uF
C70
0.1uF
C71
0.1uF
C72
0.1uF
C73
0.1uF
C74
0.1uF
C75
0.1uF
C76
0.1uF
C77
0.1uF
GND
SWD
VDD_OUT
GND
GND
NC
GND
SWDIO
SWD_CLK
USART_TX
USART_RX
RESET
FTSH-105-01-LM-DV-K
SWD_STM
PDR_ON
RST
PA13
PA14
PB6
PB5
RESET
SWD io
SWD clk
DBG tx
DBG rx
BOOT0
VCAP2
VCAP1
BYPASS_REG
STM32F777N-SYSTEM
VDD
VBAT
VDD_SDMMC
VDDUSB
VDDA
VREF+
VREF-
VSS
VSSA
C57
10uF
C58
0.1uF
Caps placed close
to VDDA pin
C60
2.2uF
C59
2.2uF
SJ1
AGND
Solder Jumper has extra
paste defined, and will
close on reflow
AGND only connects to GND at this point
STM POWER
xio
11/06/2018 09:37
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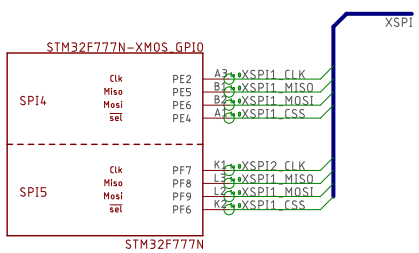

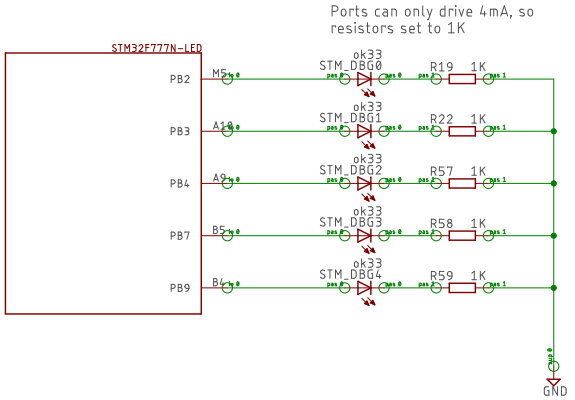

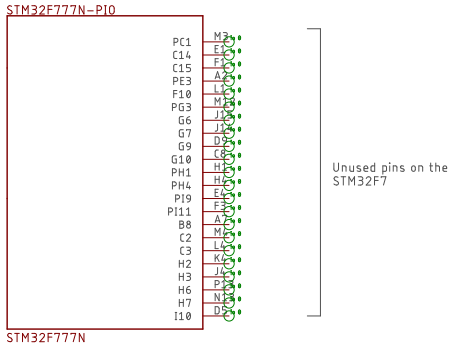

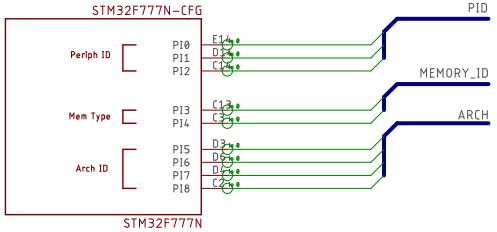

	STM Periph i/o, Debug LEDs
	xio
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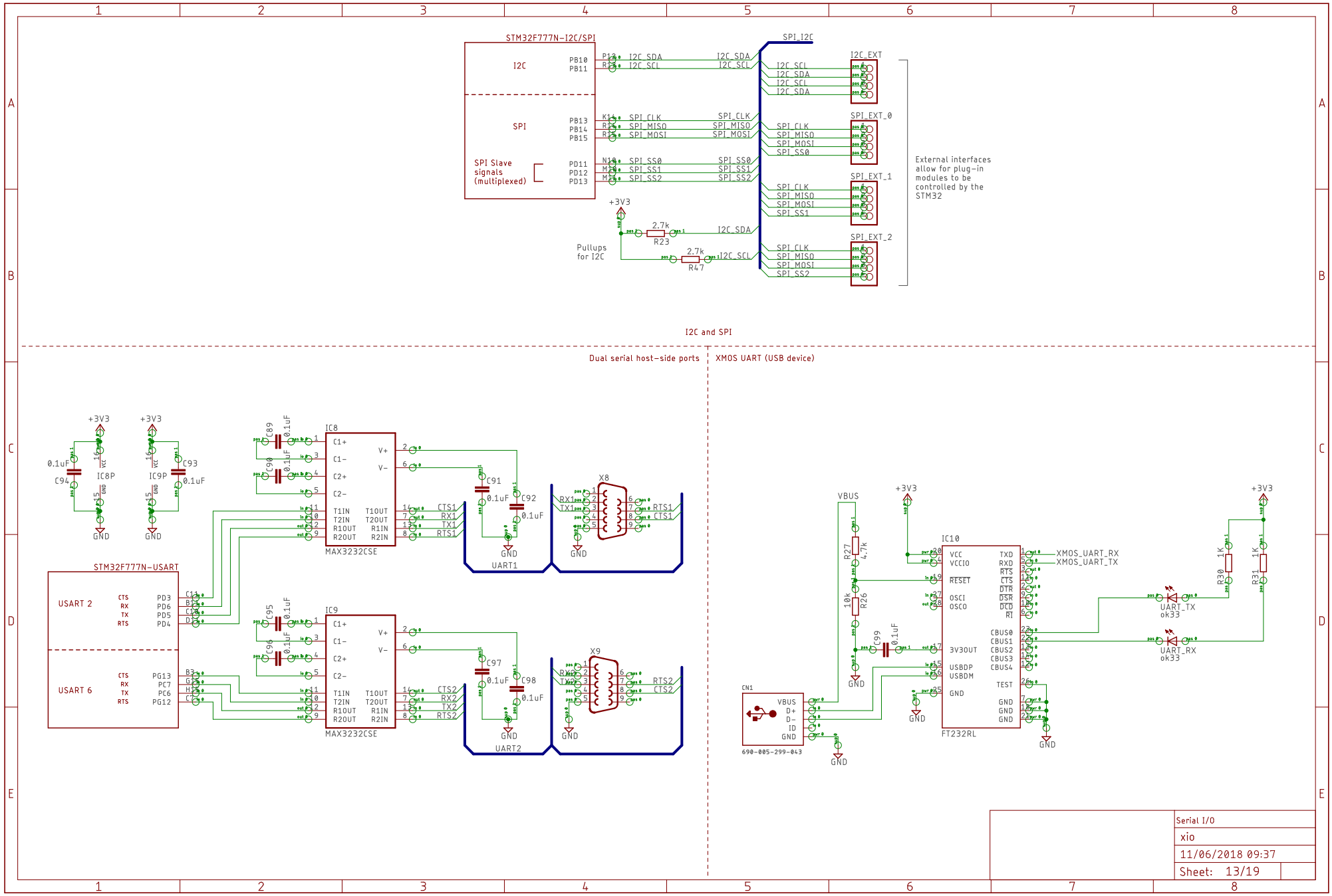
	Sheet: 12/19


STM32F777N-I2C/SPI
I2C
SPI
SPI Slave signals (multiplexed)
PB10
PB11
PB13
PB14
PB15
PD11
PD12
PD13
I2C_SDA
I2C_SCL
SPI_CLK
SPI_MISO
SPI_MOSI
SPI_SS0
SPI_SS1
SPI_SS2
SPI_I2C
I2C_EXT
SPI_EXT_0
SPI_EXT_1
SPI_EXT_2
External interfaces allow for plug-in modules to be controlled by the STM32
+3V3
2.7k
R23
R47
Pullups for I2C
I2C and SPI
Dual serial host-side ports
XMOS UART (USB device)
IC8
IC9
MAX3232CSE
C89
C90
C91
C92
C95
C96
C97
C98
0.1uF
UART1
UART2
X8
X9
RTS1
CTS1
RX1
TX1
RTS2
CTS2
RX2
TX2
STM32F777N-USART
USART 2
USART 6
IC8P
IC9P
C94
C93
IC10
FT232RL
VBUS
R27
4.7k
10k
R26
C99
CN1
690-005-299-043
XMOS_UART_RX
XMOS_UART_TX
UART_TX
UART_RX
ok33
R30
R31
1K
GND
Serial I/O
xio
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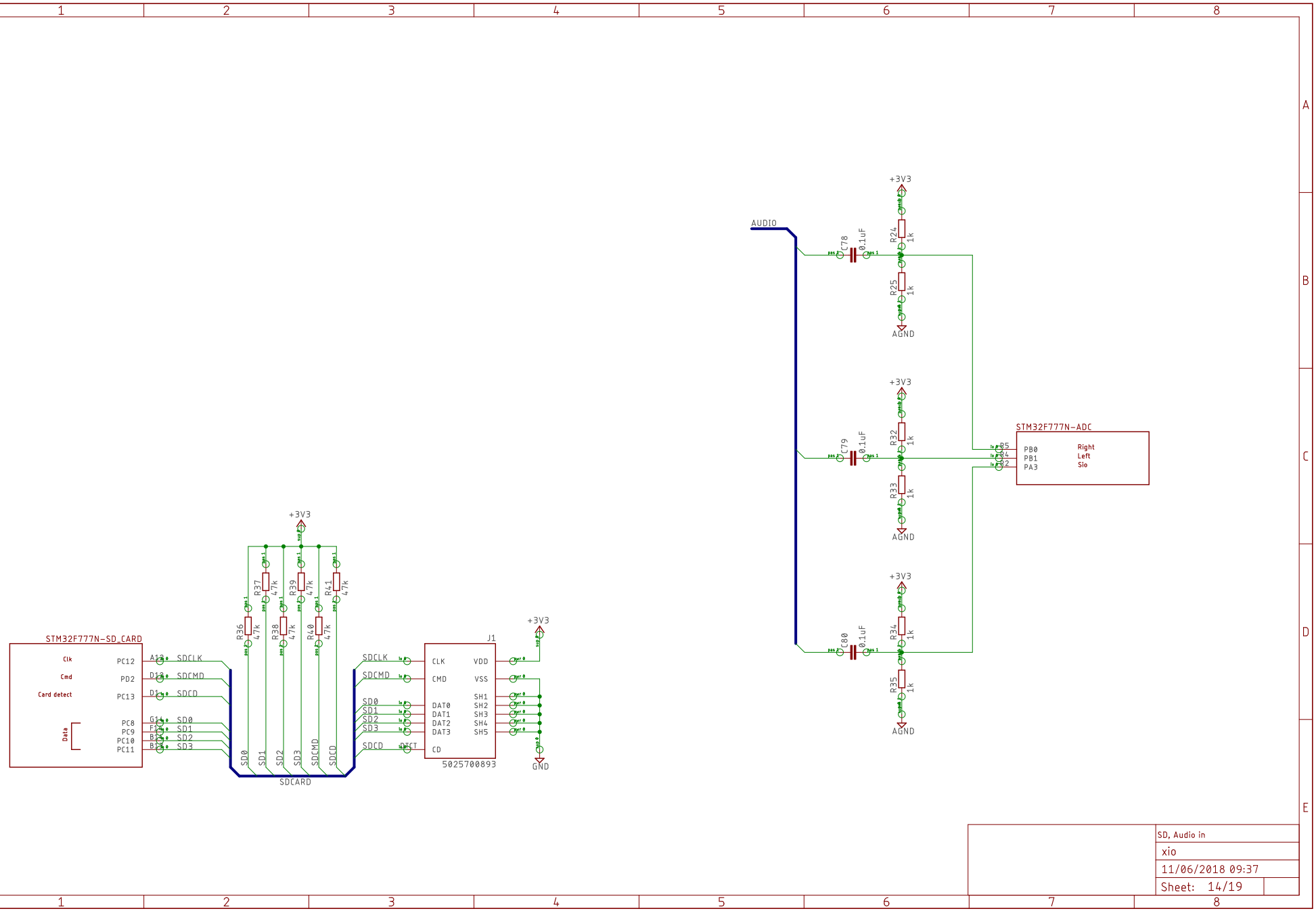
AUDIO
+3V3
R24
1k
C78
0.1uF
R25
1k
AGND
+3V3
R32
1k
C79
0.1uF
R33
1k
AGND
+3V3
R34
1k
C80
0.1uF
R35
1k
AGND
STM32F777N-ADC
PB0
PB1
PA3
Right
Left
Slo
STM32F777N-SD_CARD
Clk
Cmd
Card detect
Data
PC12
PD2
PC13
PC8
PC9
PC10
PC11
SDCLK
SDCMD
SDCD
SD0
SD1
SD2
SD3
+3V3
R36
4.7k
R37
4.7k
R38
4.7k
R39
4.7k
R40
4.7k
R41
4.7k
SDCARD
J1
CLK
CMD
DAT0
DAT1
DAT2
DAT3
VDD
VSS
SH1
SH2
SH3
SH4
SH5
CD
DFCT
5025700893
GND
SD, Audio in
xio
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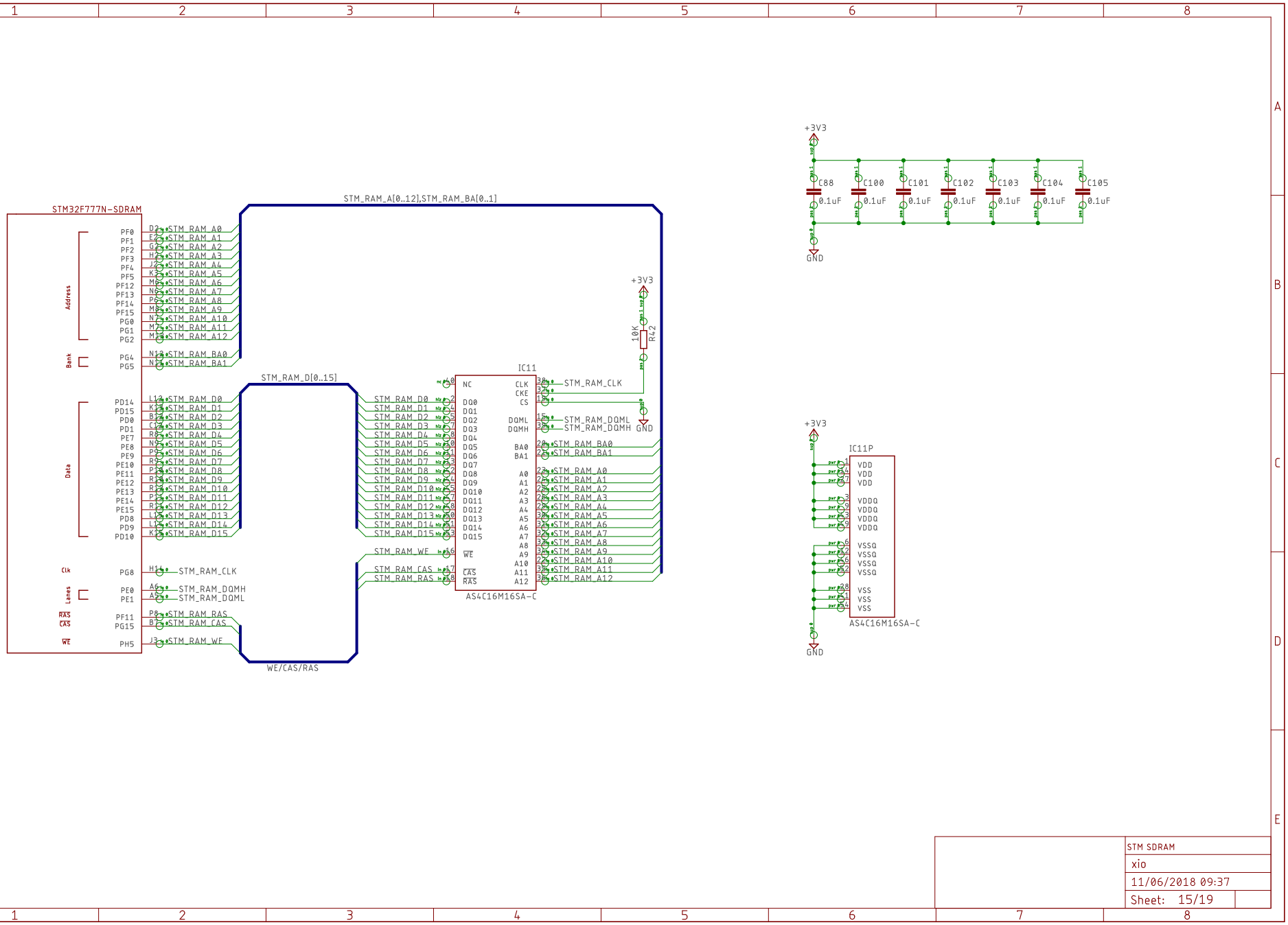
STM32F777N-SDRAM
STM_RAM_A[0..12],STM_RAM_BA[0..1]
STM_RAM_D[0..15]
WE/CAS/RAS
IC11
AS4C16M16SA-C
IC11P
AS4C16M16SA-C
+3V3
GND
10K
R42
C88 0.1uF
C100 0.1uF
C101 0.1uF
C102 0.1uF
C103 0.1uF
C104 0.1uF
C105 0.1uF
STM_RAM_CLK
STM_RAM_DQML
STM_RAM_DQMH
STM_RAM_BA0
STM_RAM_BA1
STM_RAM_A0
STM_RAM_A1
STM_RAM_A2
STM_RAM_A3
STM_RAM_A4
STM_RAM_A5
STM_RAM_A6
STM_RAM_A7
STM_RAM_A8
STM_RAM_A9
STM_RAM_A10
STM_RAM_A11
STM_RAM_A12
STM_RAM_D0
STM_RAM_D1
STM_RAM_D2
STM_RAM_D3
STM_RAM_D4
STM_RAM_D5
STM_RAM_D6
STM_RAM_D7
STM_RAM_D8
STM_RAM_D9
STM_RAM_D10
STM_RAM_D11
STM_RAM_D12
STM_RAM_D13
STM_RAM_D14
STM_RAM_D15
STM_RAM_WE
STM_RAM_CAS
STM_RAM_RAS
Address
Bank
Data
Clk
Lanes
RAS
CAS
WE
STM SDRAM
xio
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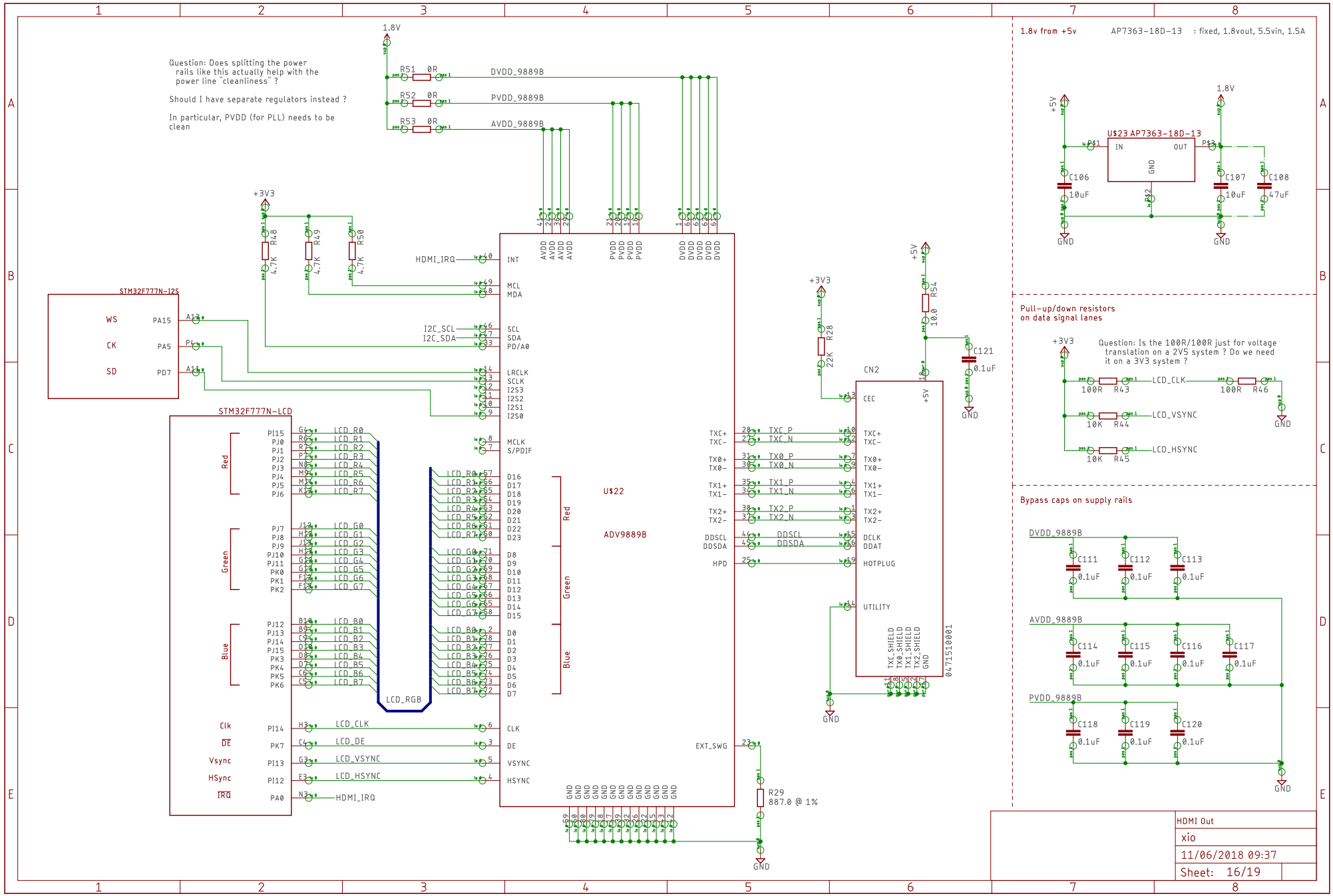
Question: Does splitting the power rails like this actually help with the power line "cleanliness" ?
Should I have separate regulators instead ?
In particular, PVDD (for PLL) needs to be clean
1.8V
R51 0R
R52 0R
R53 0R
DVDD_9889B
PVDD_9889B
AVDD_9889B
+3V3
R48 4.7K
R49 4.7K
R50 4.7K
HDMI_IRQ
I2C_SCL
I2C_SDA
MCL
MDA
SCL
SDA
PD/A0
LRCLK
SCLK
I2S3
I2S2
I2S1
I2S0
MCLK
S/PDIF
INT
U$22
ADV9889B
STM32F777N-I2S
WS
CK
SD
PA15
PA5
PD7
STM32F777N-LCD
Red
Green
Blue
LCD_R0
LCD_R1
LCD_R2
LCD_R3
LCD_R4
LCD_R5
LCD_R6
LCD_R7
LCD_G0
LCD_G1
LCD_G2
LCD_G3
LCD_G4
LCD_G5
LCD_G6
LCD_G7
LCD_B0
LCD_B1
LCD_B2
LCD_B3
LCD_B4
LCD_B5
LCD_B6
LCD_B7
LCD_RGB
Clk
DE
Vsync
HSync
IRQ
LCD_CLK
LCD_DE
LCD_VSYNC
LCD_HSYNC
CLK
DE
VSYNC
HSYNC
EXT_SWG
R29 887.0 @ 1%
CN2
TXC+
TXC-
TX0+
TX0-
TX1+
TX1-
TX2+
TX2-
DDSCL
DDSDA
HPD
UTILITY
CEC
DCLK
DDAT
HOTPLUG
TXC_SHIELD
TX0_SHIELD
TX1_SHIELD
TX2_SHIELD
GND
0471510001
R28 22K
R54 10.0
C121 0.1uF
1.8v from +5v
AP7363-18D-13 : fixed, 1.8vout, 5.5vin, 1.5A
U$23 AP7363-18D-13
IN
OUT
C106 10uF
C107 10uF
C108 47uF
Pull-up/down resistors on data signal lanes
Question: Is the 100R/100R just for voltage translation on a 2V5 system ? Do we need it on a 3V3 system ?
100R R43
100R R46
10K R44
10K R45
LCD_CLK
LCD_VSYNC
LCD_HSYNC
Bypass caps on supply rails
DVDD_9889B
AVDD_9889B
PVDD_9889B
C111 0.1uF
C112 0.1uF
C113 0.1uF
C114 0.1uF
C115 0.1uF
C116 0.1uF
C117 0.1uF
C118 0.1uF
C119 0.1uF
C120 0.1uF
HDMI Out
xio
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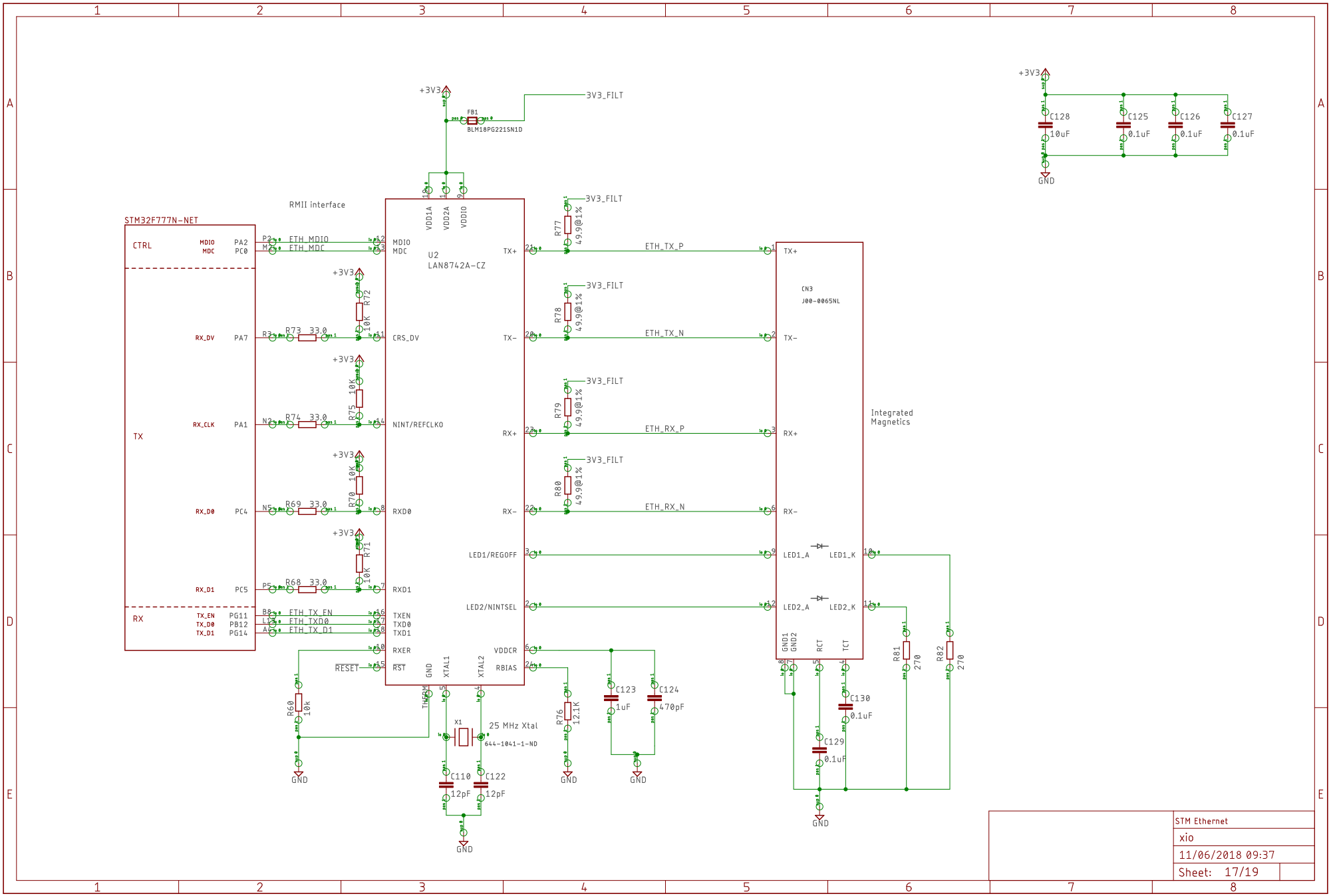
STM32F777N-NET
CTRL
TX
RX
RMII interface
U2
LAN8742A-CZ
CN3
J00-0065NL
Integrated
Magnetics
+3V3
3V3_FILT
FB1
BLM18PG221SN1D
ETH_MDIO
ETH_MDC
ETH_TX_P
ETH_TX_N
ETH_RX_P
ETH_RX_N
ETH_TX_EN
ETH_TXD0
ETH_TX_D1
RESET
25 MHz Xtal
644-1041-1-ND
GND
STM Ethernet
xio
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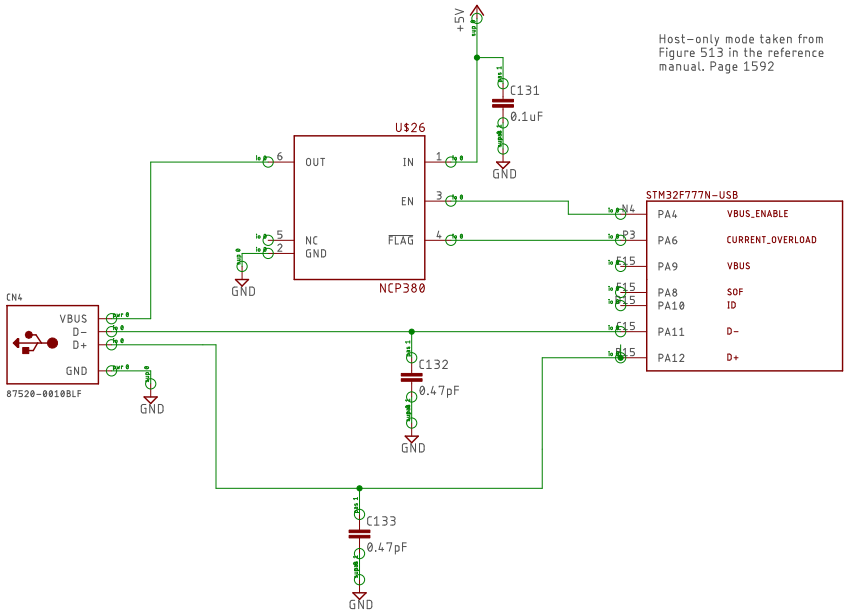

	STM USB host-only mode
	xio
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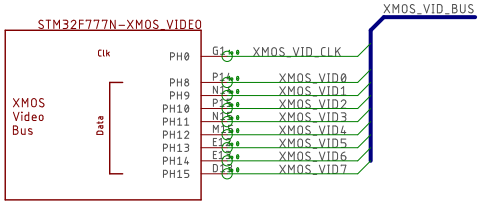

	STM VIDEO in
	xio
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