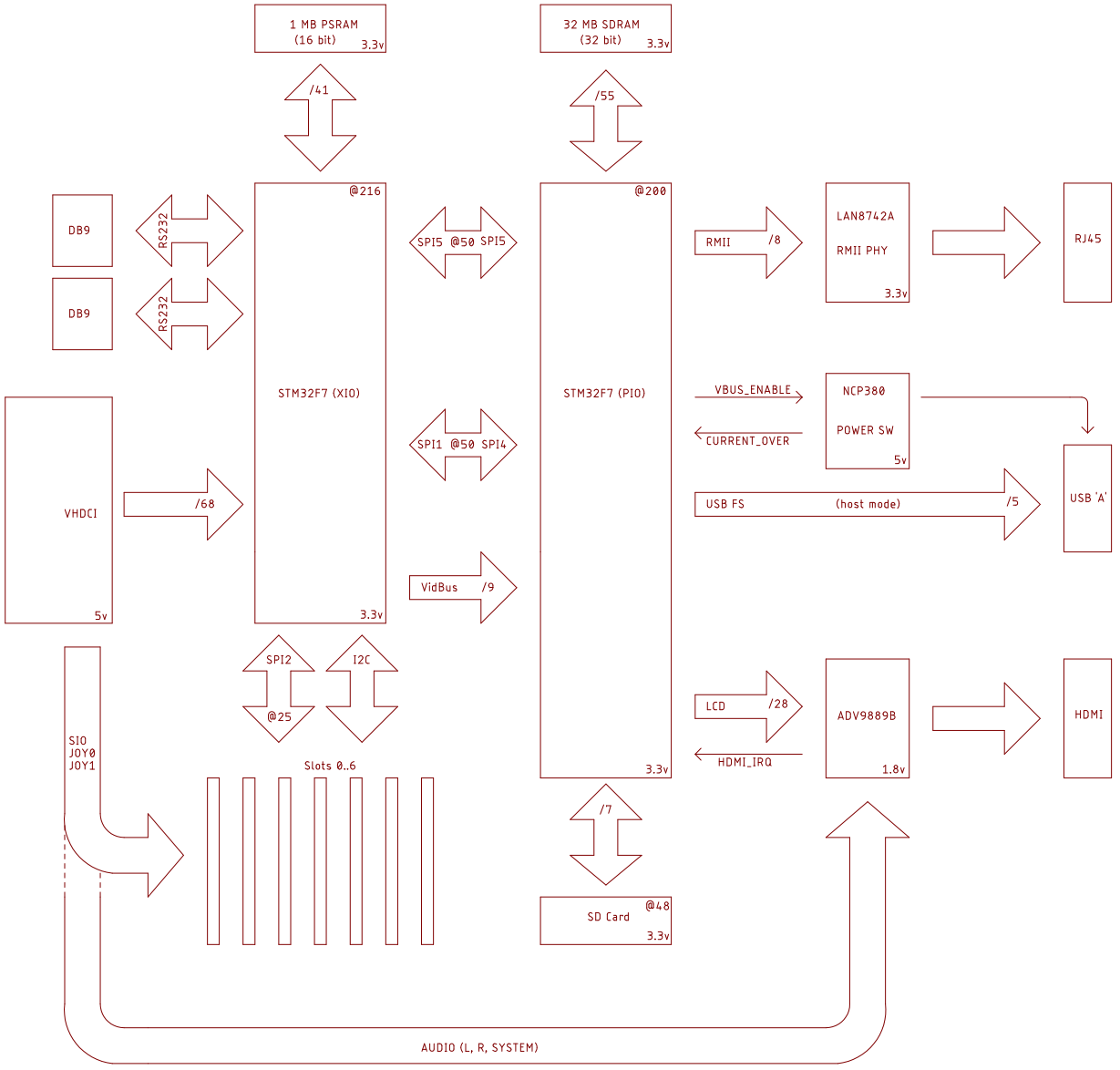


Power budgets

5v supply @ 10A
- Total power supply is 50W

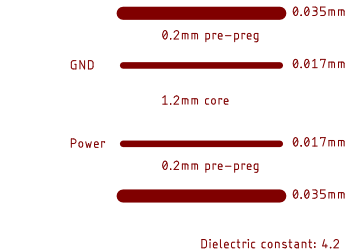
3.3v from 5V, max power provided= 1.5A / Vreg
- One Vreg per slot
- One Vreg for everything else
- Max power consumed = 4W * 7 = 28W

1.8v from 5V, max power provided = 1.5A
- Max power consumed = 4W

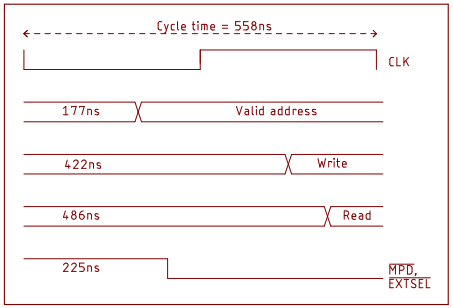
3.3v main-board current sinks (in mA)

'PIO' STM32F7	320
'XIO' STM32F7	320
IS66WV51216EBLL	25
MAX3232 x2	4
LEDs x6	20
IS42S32800J	190
LAN8742A-CZ	50
NCP380	1
Total	910

Layer stack-up



Dielectric constant: 4.2



Block Diagram	
xio	
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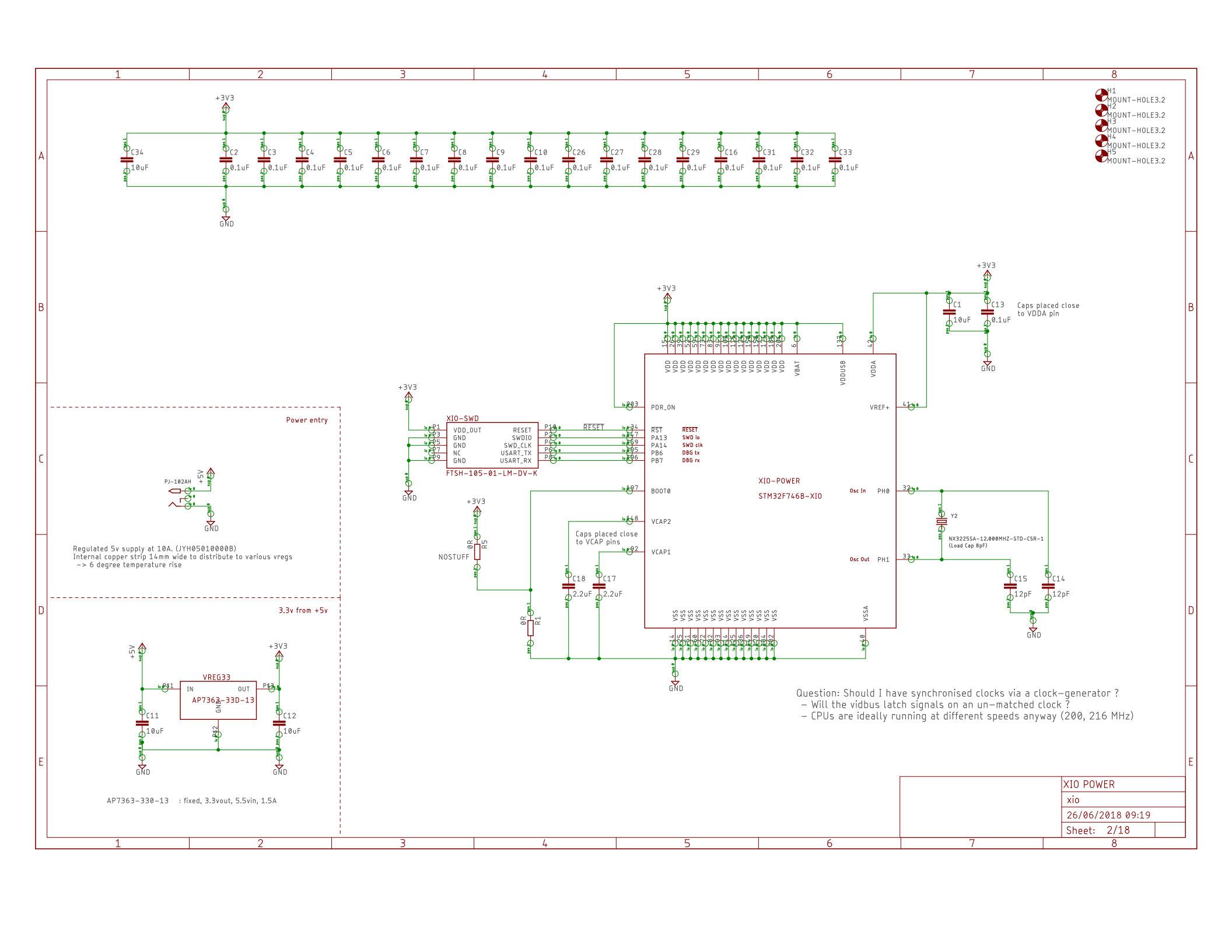
+3V3
C34 10uF
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
C16 0.1uF
C31 0.1uF
C32 0.1uF
C33 0.1uF
GND
H1 MOUNT-HOLE3.2
H2 MOUNT-HOLE3.2
H3 MOUNT-HOLE3.2
H4 MOUNT-HOLE3.2
H5 MOUNT-HOLE3.2
Power entry
PJ-102AH
+5V
GND
Regulated 5v supply at 10A. (JYH05010000B)
Internal copper strip 14mm wide to distribute to various vregs
-> 6 degree temperature rise
3.3v from +5v
VREG33
IN
OUT
GND
AP7363-33D-13
C11 10uF
C12 10uF
AP7363-330-13 : fixed, 3.3vout, 5.5vin, 1.5A
XIO-SWD
VDD_OUT
GND
GND
NC
GND
RESET
SWDIO
SWD_CLK
USART_TX
USART_RX
FTSH-105-01-LM-DV-K
RESET
NOSTUFF
0R R5
0R R1
C18 2.2uF
C17 2.2uF
Caps placed close to VCAP pins
XIO-POWER
STM32F746B-XIO
PDR_ON
BOOT0
VCAP2
VCAP1
VBAT
VDDUSB
VDDA
VREF+
PH0
PH1
RST
PA13
PA14
PB6
PB7
RESET
SWD io
SWD clk
DBG tx
DBG rx
Osc In
Osc Out
C1 10uF
C13 0.1uF
Caps placed close to VDDA pin
Y2
NX3225SA-12.000MHZ-STD-CSR-1
(Load Cap 8pF)
C15 12pF
C14 12pF
Question: Should I have synchronised clocks via a clock-generator ?
– Will the vidbus latch signals on an un-matched clock ?
– CPUs are ideally running at different speeds anyway (200, 216 MHz)
XIO POWER
xio
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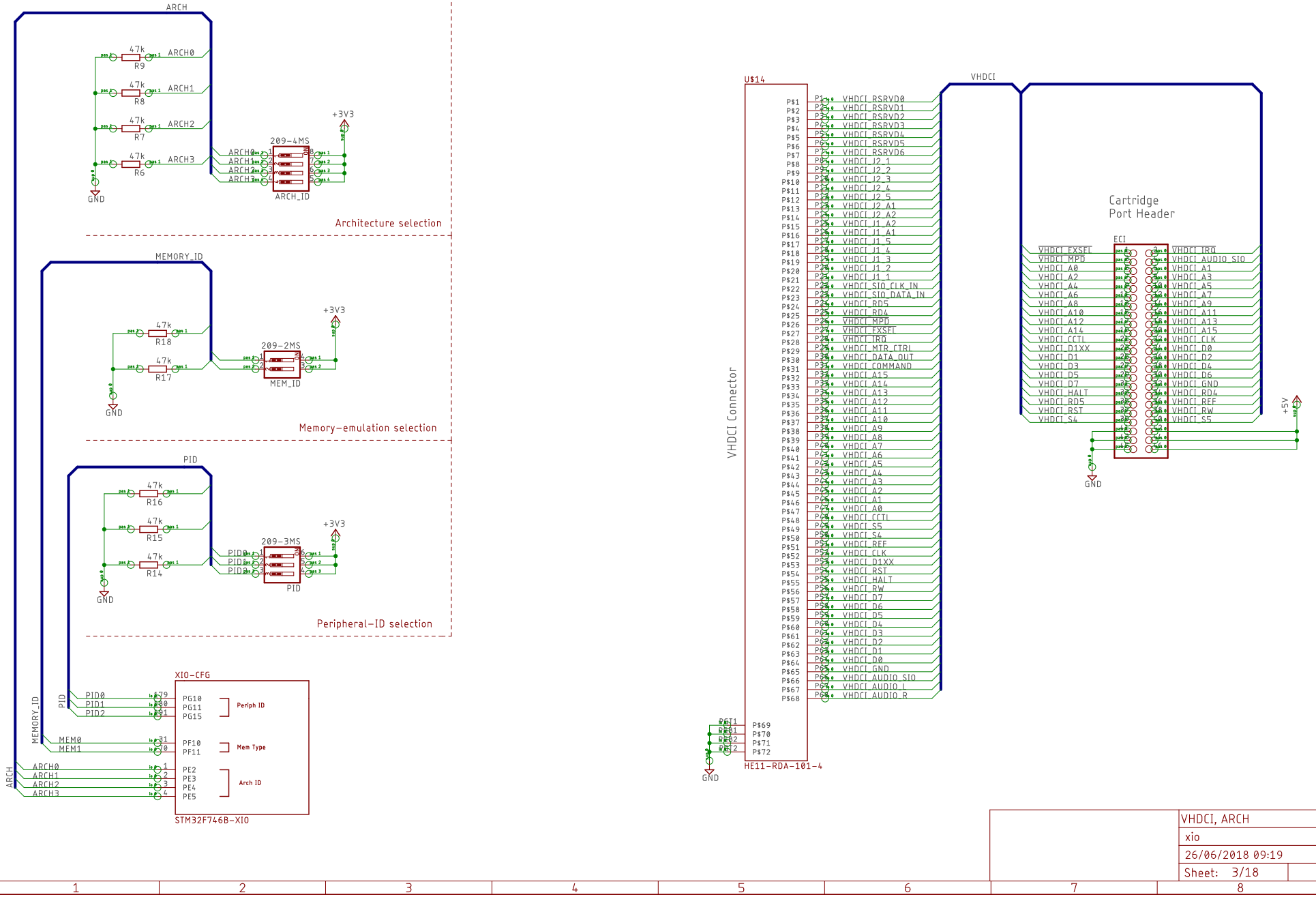
ARCH
47k
R9
ARCH0
47k
R8
ARCH1
47k
R7
ARCH2
47k
R6
ARCH3
+3V3
209-4MS
ARCH_ID
GND
Architecture selection
MEMORY_ID
47k
R18
47k
R17
+3V3
209-2MS
MEM_ID
GND
Memory-emulation selection
PID
47k
R16
47k
R15
47k
R14
+3V3
209-3MS
PID
GND
Peripheral-ID selection
XIO-CFG
PID0
PID1
PID2
PG10
PG11
PG15
Periph ID
MEM0
MEM1
PF10
PF11
Mem Type
ARCH0
ARCH1
ARCH2
ARCH3
PE2
PE3
PE4
PE5
Arch ID
STM32F746B-XIO
U$14
VHDCI Connector
HE11-RDA-101-4
VHDCI
Cartridge
Port Header
ECI
+5V
GND
VHDCI, ARCH
xio
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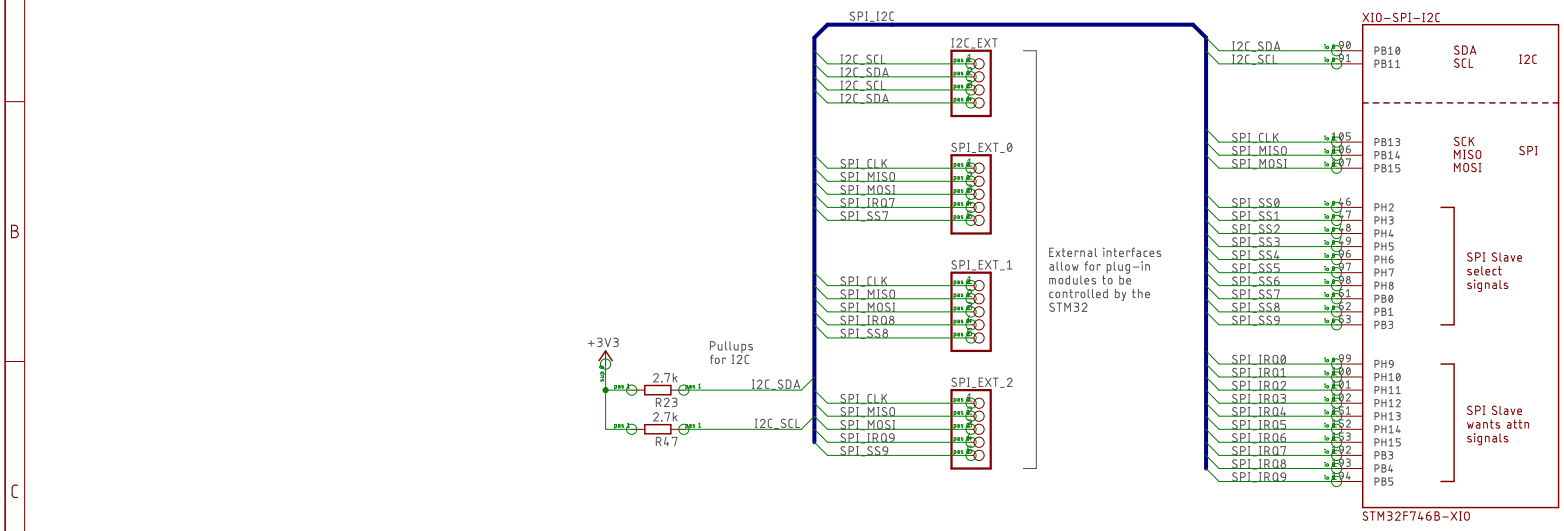
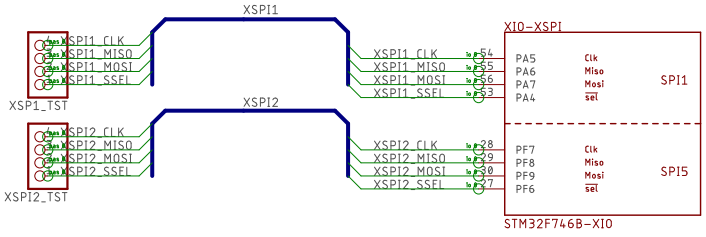


Slot/Ext I2C and SPI
SPI link runs at up to 25MHz

Inter-CPU SPI
Both at up to 50MHz



	XIO SPI, I2C
	xio
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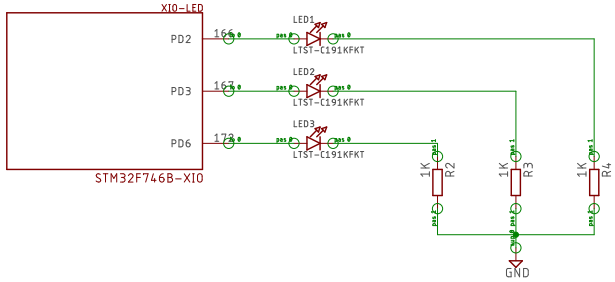
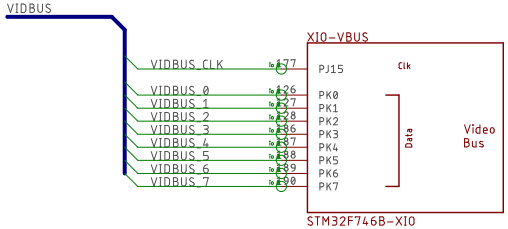
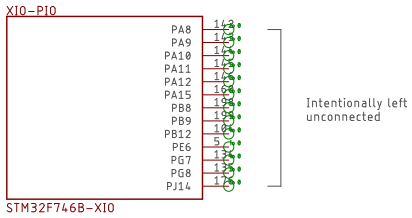




Debug LEDs

Video bus out

Unused pins



	LEDs, Video-bus, unused
	xio
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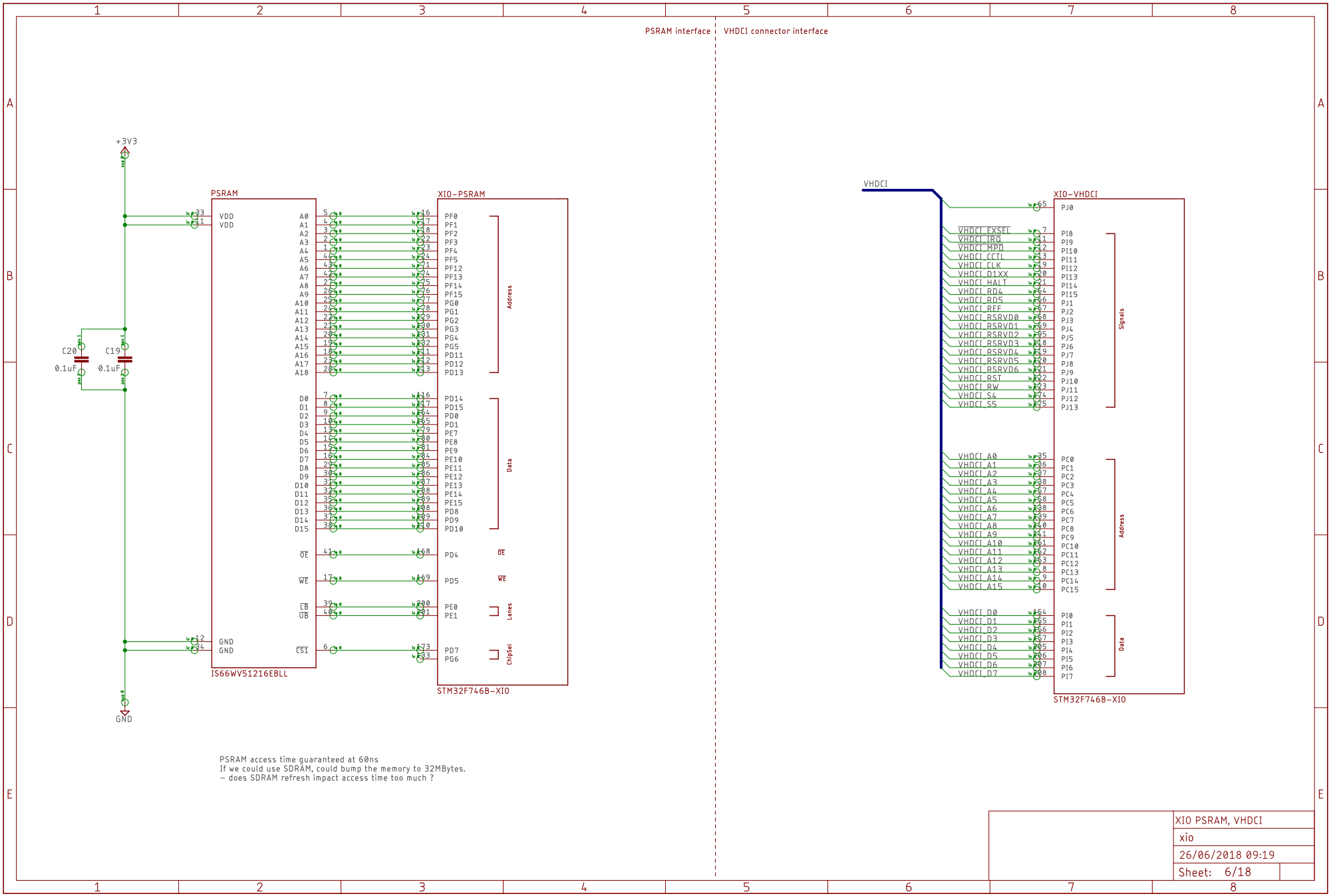
PSRAM interface
VHDCI connector interface
+3V3
PSRAM
XIO-PSRAM
VDD
VDD
GND
GND
C20
0.1uF
C19
0.1uF
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
OE
WE
LB
UB
CS1
PF0
PF1
PF2
PF3
PF4
PF5
PF12
PF13
PF14
PF15
PG0
PG1
PG2
PG3
PG4
PG5
PD11
PD12
PD13
PD14
PD15
PD0
PD1
PE7
PE8
PE9
PE10
PE11
PE12
PE13
PE14
PE15
PD8
PD9
PD10
PD4
PD5
PE0
PE1
PD7
PG6
Address
Data
OE
WE
Lanes
ChipSel
IS66WV51216EBLL
STM32F746B-XIO
VHDCI
XIO-VHDCI
PJ0
VHDCI_EXSET
VHDCI_IRQ
VHDCI_MPD
VHDCI_CCTL
VHDCI_CLK
VHDCI_D1XX
VHDCI_HALT
VHDCI_RD4
VHDCI_RD5
VHDCI_REF
VHDCI_RSRVD0
VHDCI_RSRVD1
VHDCI_RSRVD2
VHDCI_RSRVD3
VHDCI_RSRVD4
VHDCI_RSRVD5
VHDCI_RSRVD6
VHDCI_RST
VHDCI_RW
VHDCI_S4
VHDCI_S5
PI8
PI9
PI10
PI11
PI12
PI13
PI14
PI15
PJ1
PJ2
PJ3
PJ4
PJ5
PJ6
PJ7
PJ8
PJ9
PJ10
PJ11
PJ12
PJ13
Signals
VHDCI_A0
VHDCI_A1
VHDCI_A2
VHDCI_A3
VHDCI_A4
VHDCI_A5
VHDCI_A6
VHDCI_A7
VHDCI_A8
VHDCI_A9
VHDCI_A10
VHDCI_A11
VHDCI_A12
VHDCI_A13
VHDCI_A14
VHDCI_A15
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
PC12
PC13
PC14
PC15
Address
VHDCI_D0
VHDCI_D1
VHDCI_D2
VHDCI_D3
VHDCI_D4
VHDCI_D5
VHDCI_D6
VHDCI_D7
PI0
PI1
PI2
PI3
PI4
PI5
PI6
PI7
Data
STM32F746B-XIO
PSRAM access time guaranteed at 60ns
If we could use SDRAM, could bump the memory to 32MBytes.
– does SDRAM refresh impact access time too much ?
XIO PSRAM, VHDCI
xio
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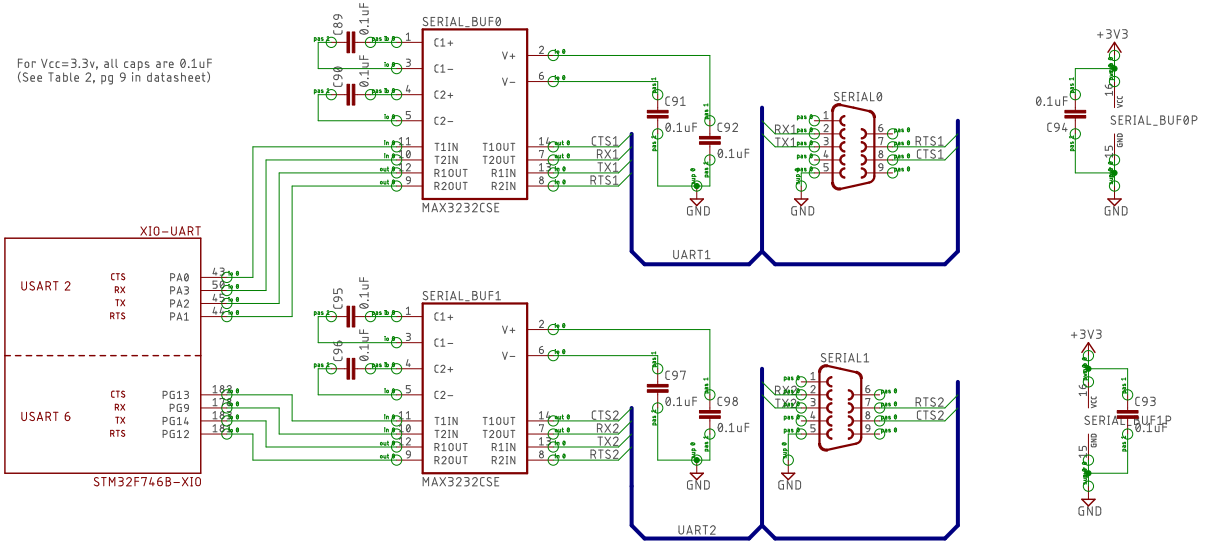

	XIO Serial I/O
	xio
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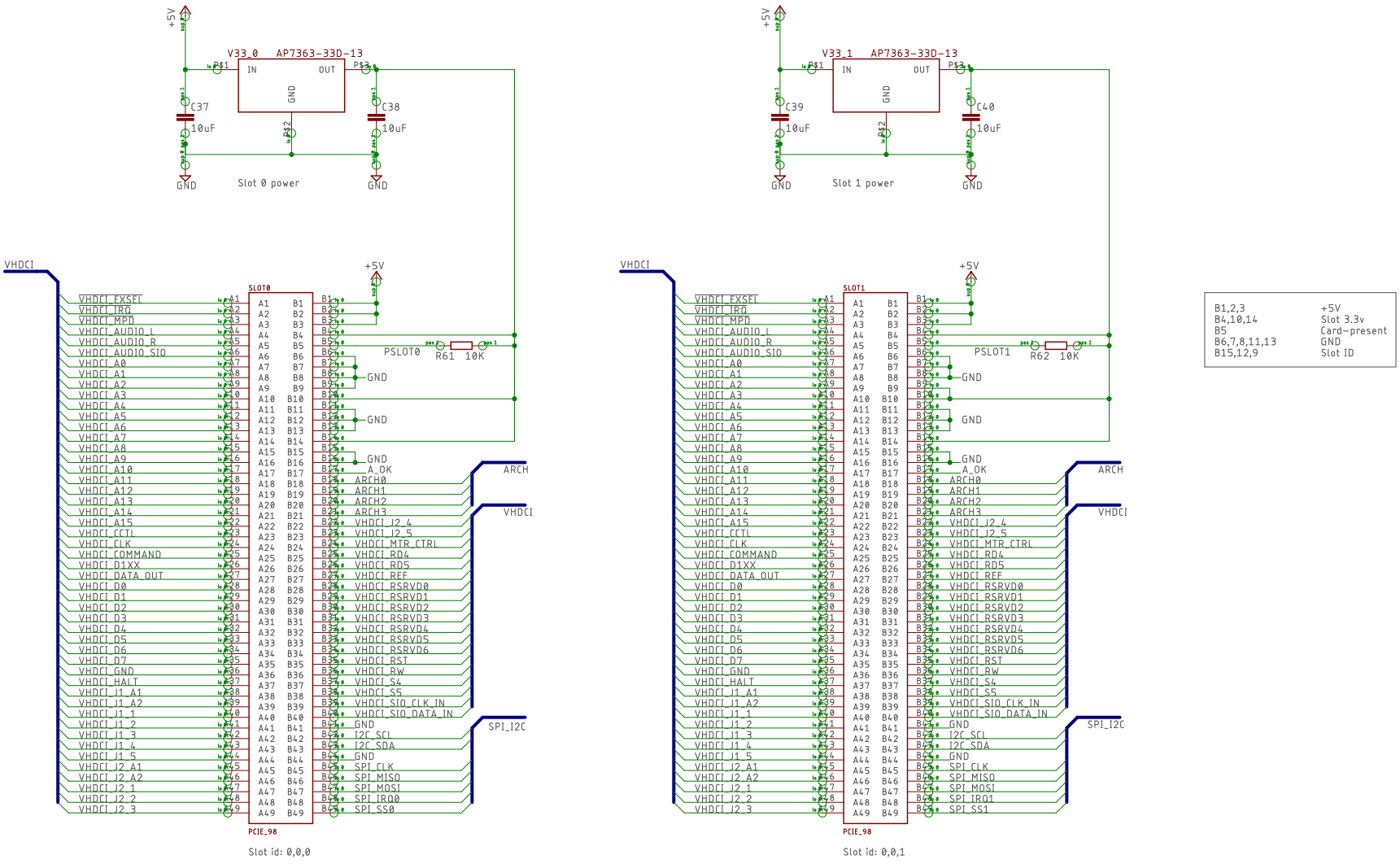
V33_0 AP7363-33D-13
V33_1 AP7363-33D-13
IN
OUT
GND
+5V
C37 10uF
C38 10uF
C39 10uF
C40 10uF
R62
Slot 0 power
Slot 1 power
VHDCI
SLOT0
SLOT1
PCIE_98
PSLOT0
PSLOT1
R61 10K
R62 10K
VHDCI_EXSET
VHDCI_IRQ
VHDCI_MPD
VHDCI_AUDIO_L
VHDCI_AUDIO_R
VHDCI_AUDIO_SIO
VHDCI_A0
VHDCI_A1
VHDCI_A2
VHDCI_A3
VHDCI_A4
VHDCI_A5
VHDCI_A6
VHDCI_A7
VHDCI_A8
VHDCI_A9
VHDCI_A10
VHDCI_A11
VHDCI_A12
VHDCI_A13
VHDCI_A14
VHDCI_A15
VHDCI_CCTL
VHDCI_CLK
VHDCI_COMMAND
VHDCI_D1XX
VHDCI_DATA_OUT
VHDCI_D0
VHDCI_D1
VHDCI_D2
VHDCI_D3
VHDCI_D4
VHDCI_D5
VHDCI_D6
VHDCI_D7
VHDCI_GND
VHDCI_HALT
VHDCI_J1_A1
VHDCI_J1_A2
VHDCI_J1_1
VHDCI_J1_2
VHDCI_J1_3
VHDCI_J1_4
VHDCI_J1_5
VHDCI_J2_A1
VHDCI_J2_A2
VHDCI_J2_1
VHDCI_J2_2
VHDCI_J2_3
A_OK
ARCH0
ARCH1
ARCH2
ARCH3
VHDCI_J2_4
VHDCI_J2_5
VHDCI_MTR_CTRL
VHDCI_RD4
VHDCI_RD5
VHDCI_REF
VHDCI_RSRVD0
VHDCI_RSRVD1
VHDCI_RSRVD2
VHDCI_RSRVD3
VHDCI_RSRVD4
VHDCI_RSRVD5
VHDCI_RSRVD6
VHDCI_RST
VHDCI_RW
VHDCI_S4
VHDCI_S5
VHDCI_SIO_CLK_IN
VHDCI_SIO_DATA_IN
I2C_SCL
I2C_SDA
SPI_CLK
SPI_MISO
SPI_MOSI
SPI_IRQ0
SPI_IRQ1
SPI_SS0
SPI_SS1
ARCH
VHDCI
SPI_I2C
Slot id: 0,0,0
Slot id: 0,0,1
B1,2,3 +5V
B4,10,14 Slot 3.3v
B5 Card-present
B6,7,8,11,13 GND
B15,12,9 Slot ID
Slots 0,1
xio
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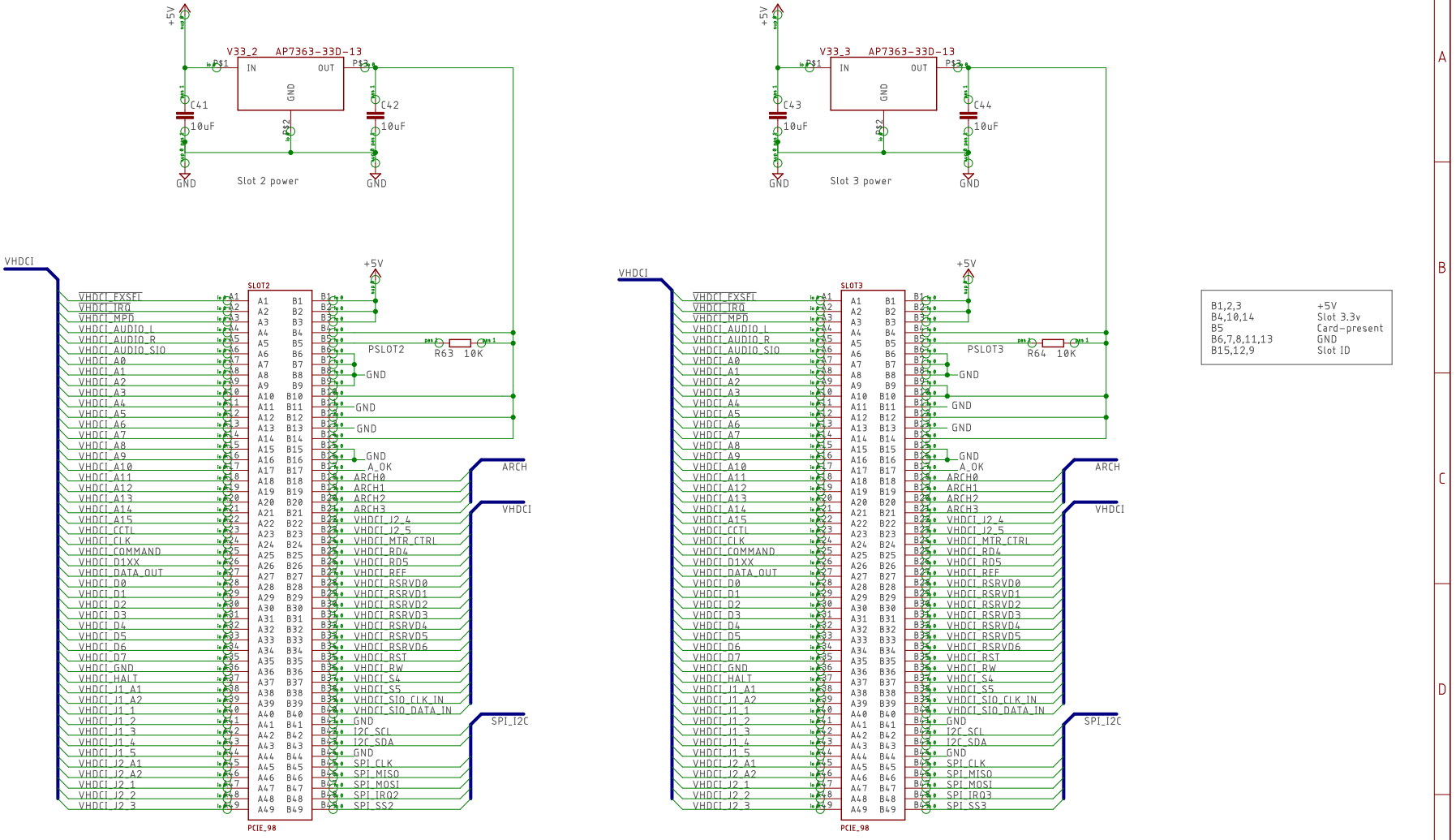
Sheet: 8/18



B1,2,3	+5V
B4,10,14	Slot 3.3v
B5	Card-present
B6,7,8,11,13	GND
B15,12,9	Slot ID

Slots 2,3	
xio	
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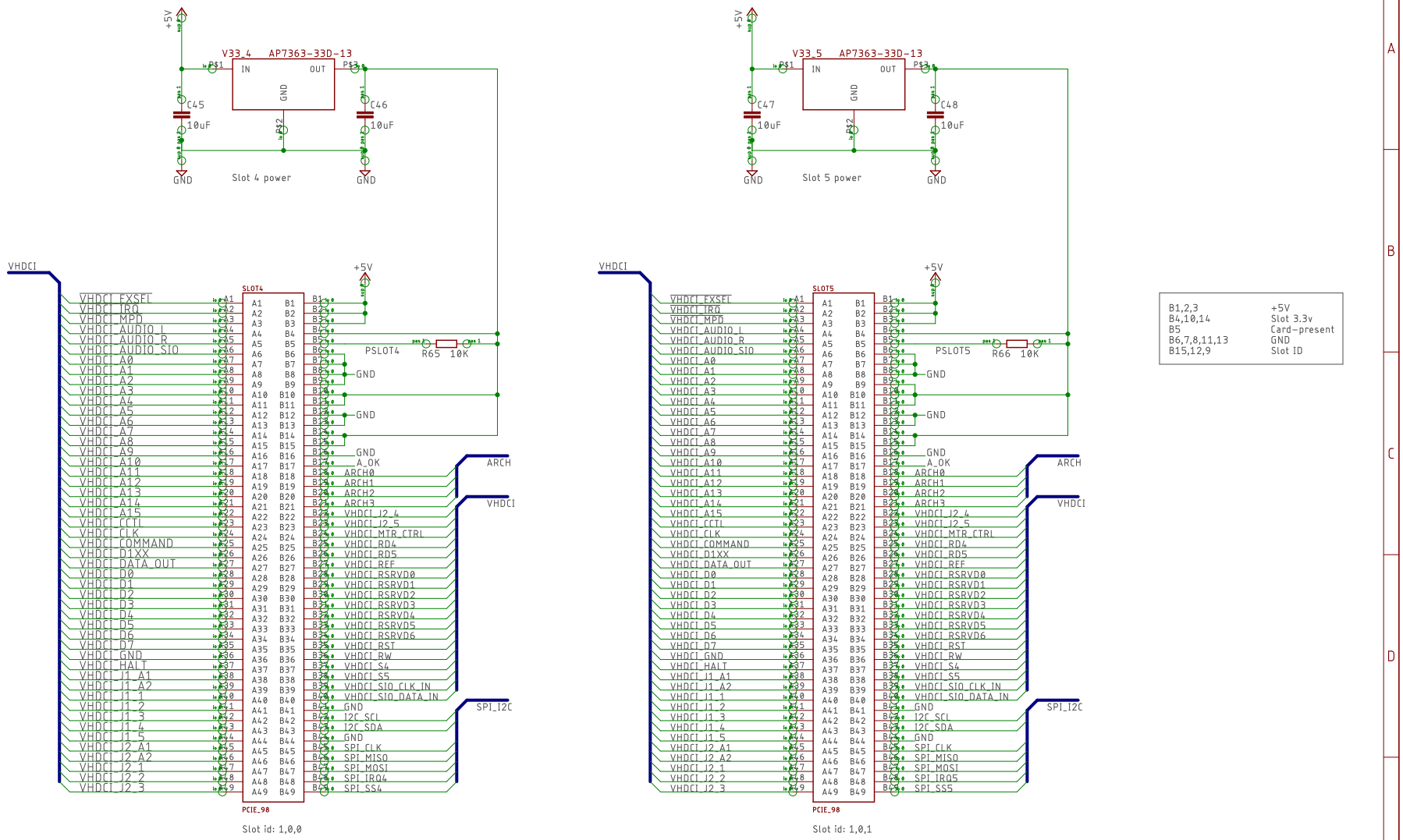
V33_4 AP7363-33D-13
IN
OUT
GND
C45
10uF
C46
10uF
Slot 4 power
V33_5 AP7363-33D-13
C47
10uF
C48
10uF
Slot 5 power
+5V
GND
VHDCI
SLOT4
SLOT5
PSLOT4
PSLOT5
R65 10K
R66 10K
VHDCI_FXSET
VHDCI_IRQ
VHDCI_MPD
VHDCI_AUDIO_L
VHDCI_AUDIO_R
VHDCI_AUDIO_SIO
VHDCI_A0
VHDCI_A1
VHDCI_A2
VHDCI_A3
VHDCI_A4
VHDCI_A5
VHDCI_A6
VHDCI_A7
VHDCI_A8
VHDCI_A9
VHDCI_A10
VHDCI_A11
VHDCI_A12
VHDCI_A13
VHDCI_A14
VHDCI_A15
VHDCI_CCTL
VHDCI_CLK
VHDCI_COMMAND
VHDCI_D1XX
VHDCI_DATA_OUT
VHDCI_D0
VHDCI_D1
VHDCI_D2
VHDCI_D3
VHDCI_D4
VHDCI_D5
VHDCI_D6
VHDCI_D7
VHDCI_GND
VHDCI_HALT
VHDCI_J1_A1
VHDCI_J1_A2
VHDCI_J1_1
VHDCI_J1_2
VHDCI_J1_3
VHDCI_J1_4
VHDCI_J1_5
VHDCI_J2_A1
VHDCI_J2_A2
VHDCI_J2_1
VHDCI_J2_2
VHDCI_J2_3
A_OK
ARCH0
ARCH1
ARCH2
ARCH3
VHDCI_J2_4
VHDCI_J2_5
VHDCI_MTR_CTRL
VHDCI_RD4
VHDCI_RD5
VHDCI_REF
VHDCI_RSRVD0
VHDCI_RSRVD1
VHDCI_RSRVD2
VHDCI_RSRVD3
VHDCI_RSRVD4
VHDCI_RSRVD5
VHDCI_RSRVD6
VHDCI_RST
VHDCI_RW
VHDCI_S4
VHDCI_S5
VHDCI_SIO_CLK_IN
VHDCI_SIO_DATA_IN
I2C_SCL
I2C_SDA
SPI_CLK
SPI_MISO
SPI_MOSI
SPI_IRQ4
SPI_SS4
SPI_IRQ5
SPI_SS5
ARCH
VHDCI
SPI_I2C
PCIE_98
Slot id: 1,0,0
Slot id: 1,0,1
B1,2,3 +5V
B4,10,14 Slot 3.3v
B5 Card-present
B6,7,8,11,13 GND
B15,12,9 Slot ID
Slots 4,5
xio
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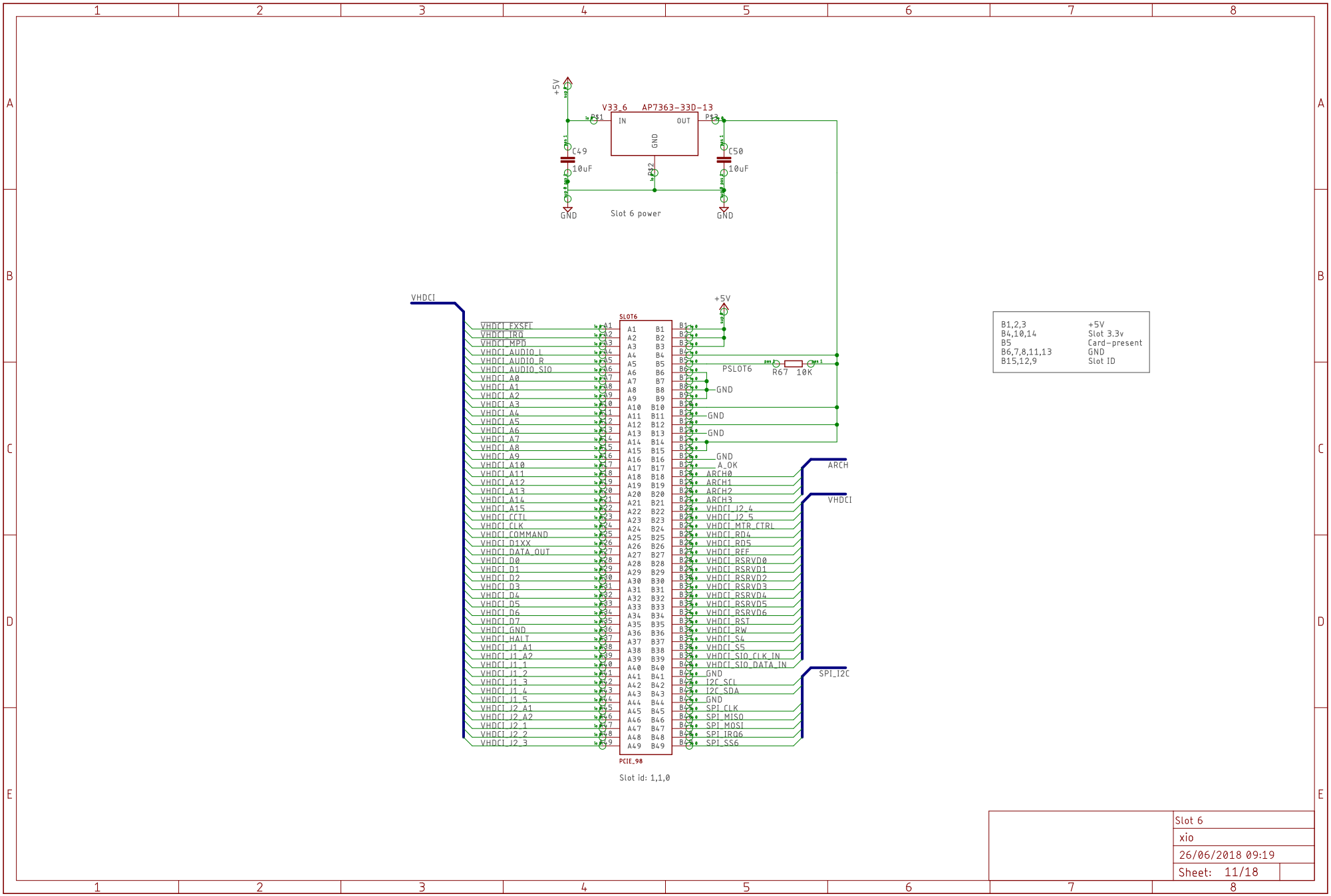
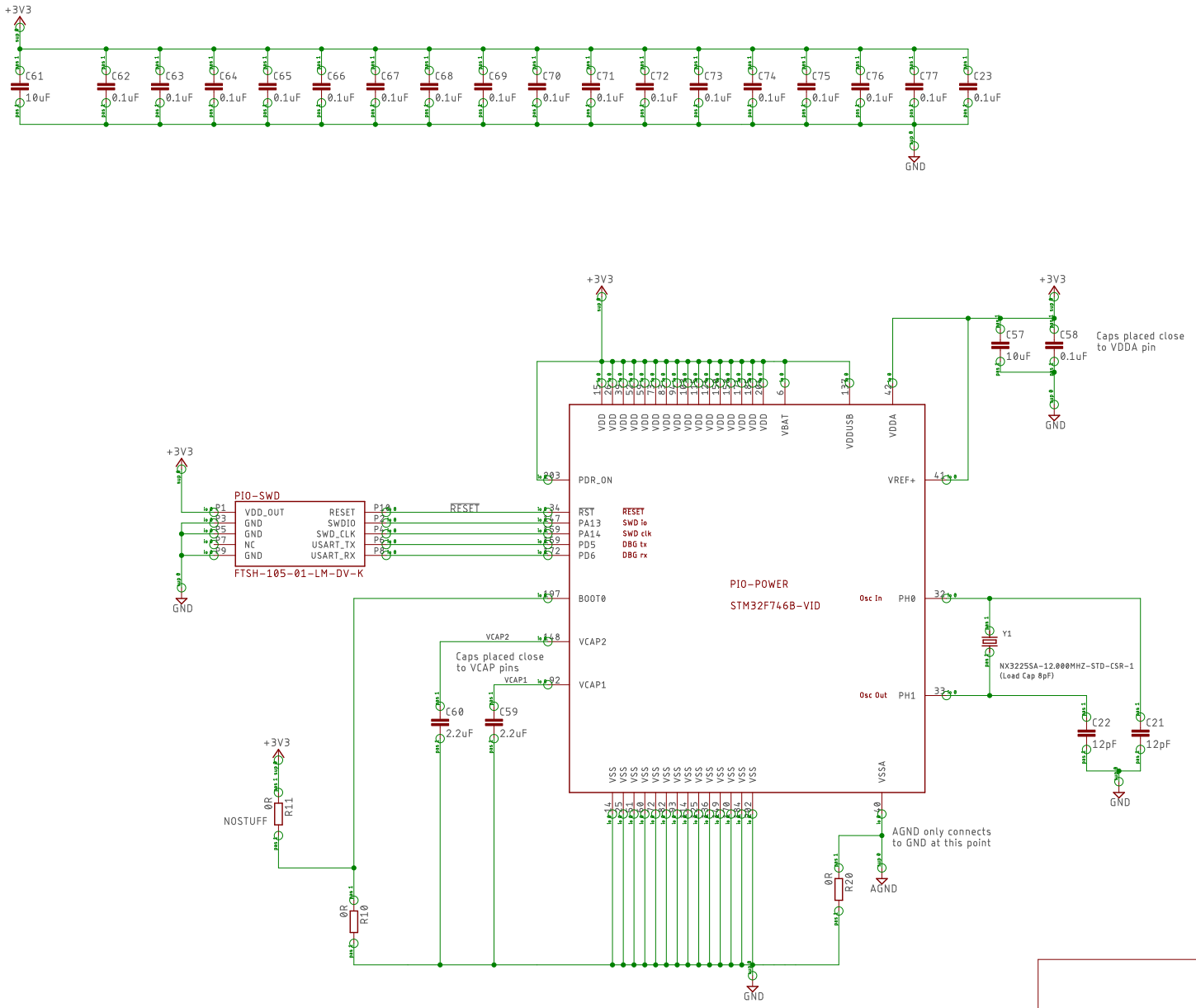
Sheet: 10/18


V33_6 AP7363-33D-13
IN
OUT
GND
C49
10uF
C50
10uF
+5V
GND
GND
Slot 6 power
VHDCI
SLOT6
PSLOT6
R67 10K
+5V
GND
GND
GND
GND
A_OK
ARCH
ARCH0
ARCH1
ARCH2
ARCH3
VHDCI
VHDCI_J2_4
VHDCI_J2_5
VHDCI_MTR_CTRL
VHDCI_RD4
VHDCI_RD5
VHDCI_REF
VHDCI_RSRVD0
VHDCI_RSRVD1
VHDCI_RSRVD2
VHDCI_RSRVD3
VHDCI_RSRVD4
VHDCI_RSRVD5
VHDCI_RSRVD6
VHDCI_RST
VHDCI_RW
VHDCI_S4
VHDCI_S5
VHDCI_SIO_CLK_IN
VHDCI_SIO_DATA_IN
SPI_I2C
GND
I2C_SCL
I2C_SDA
GND
SPI_CLK
SPI_MISO
SPI_MOSI
SPI_IRQ6
SPI_SS6
VHDCI_EXSET
VHDCI_IRQ
VHDCI_MPD
VHDCI_AUDIO_L
VHDCI_AUDIO_R
VHDCI_AUDIO_SIO
VHDCI_A0
VHDCI_A1
VHDCI_A2
VHDCI_A3
VHDCI_A4
VHDCI_A5
VHDCI_A6
VHDCI_A7
VHDCI_A8
VHDCI_A9
VHDCI_A10
VHDCI_A11
VHDCI_A12
VHDCI_A13
VHDCI_A14
VHDCI_A15
VHDCI_CCTL
VHDCI_CLK
VHDCI_COMMAND
VHDCI_D1XX
VHDCI_DATA_OUT
VHDCI_D0
VHDCI_D1
VHDCI_D2
VHDCI_D3
VHDCI_D4
VHDCI_D5
VHDCI_D6
VHDCI_D7
VHDCI_GND
VHDCI_HALT
VHDCI_J1_A1
VHDCI_J1_A2
VHDCI_J1_1
VHDCI_J1_2
VHDCI_J1_3
VHDCI_J1_4
VHDCI_J1_5
VHDCI_J2_A1
VHDCI_J2_A2
VHDCI_J2_1
VHDCI_J2_2
VHDCI_J2_3
PCIE_98
Slot id: 1,1,0
B1,2,3 +5V
B4,10,14 Slot 3.3v
B5 Card-present
B6,7,8,11,13 GND
B15,12,9 Slot ID
Slot 6
xio
26/06/2018 09:19
Sheet: 11/18



PIO POWER	
xio	
26/06/2018 09:19	
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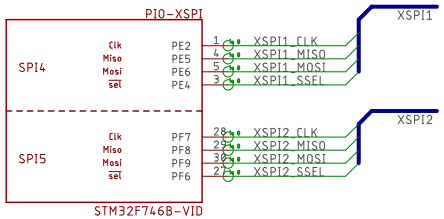
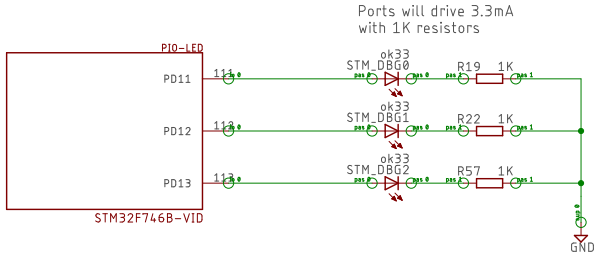
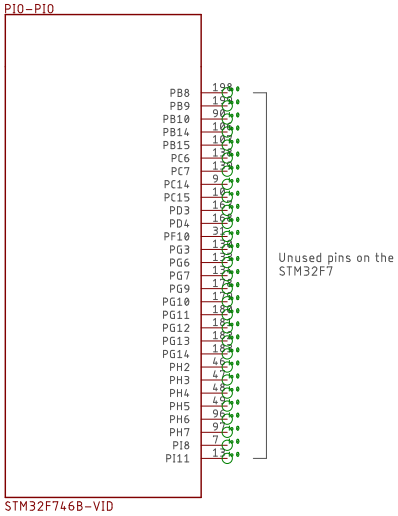


XSPI to XIO



LEDs

Unused pins



	PIO LEDs, XSPI to XIO, Unused
	xio
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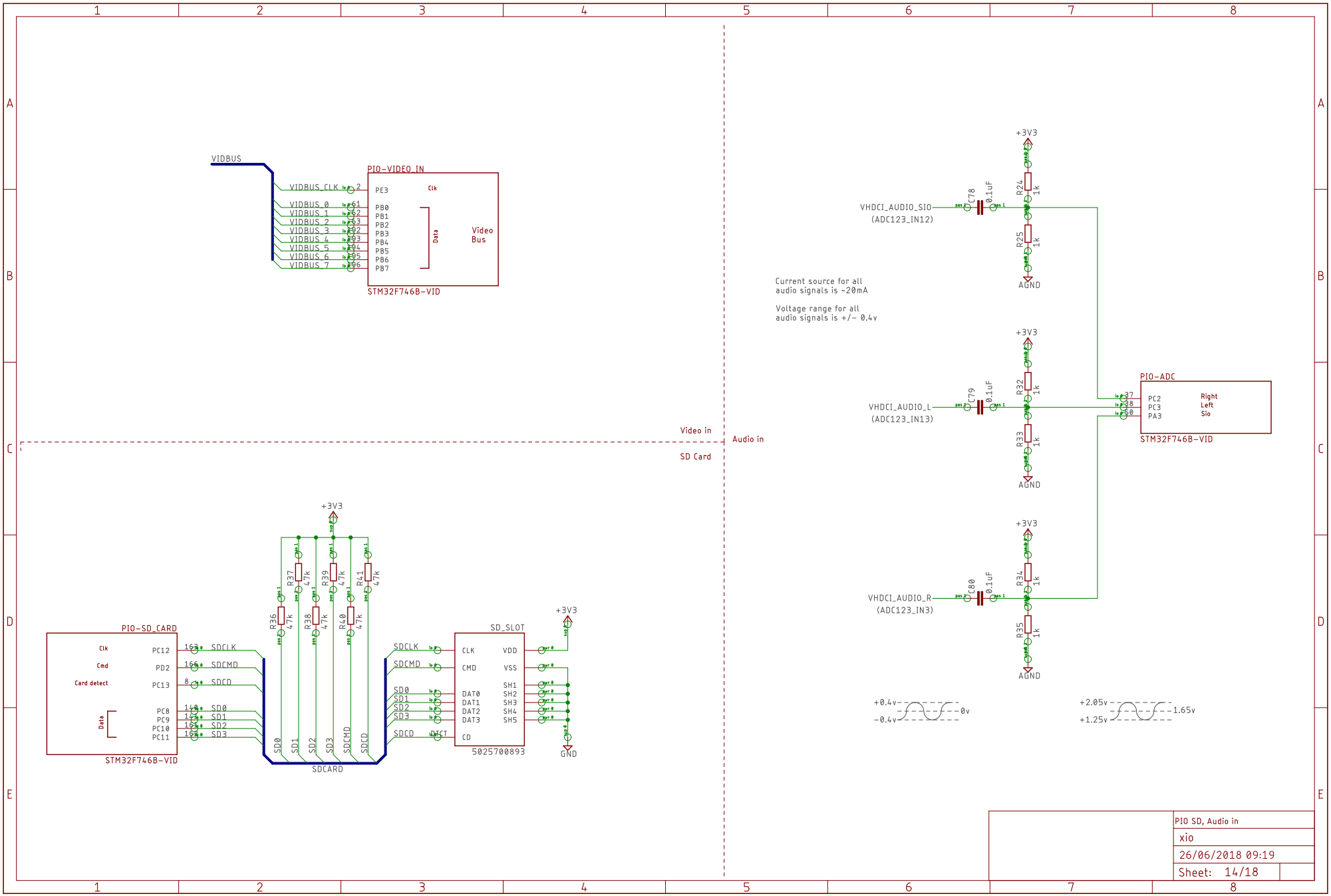

	PIO SD, Audio in
	xio
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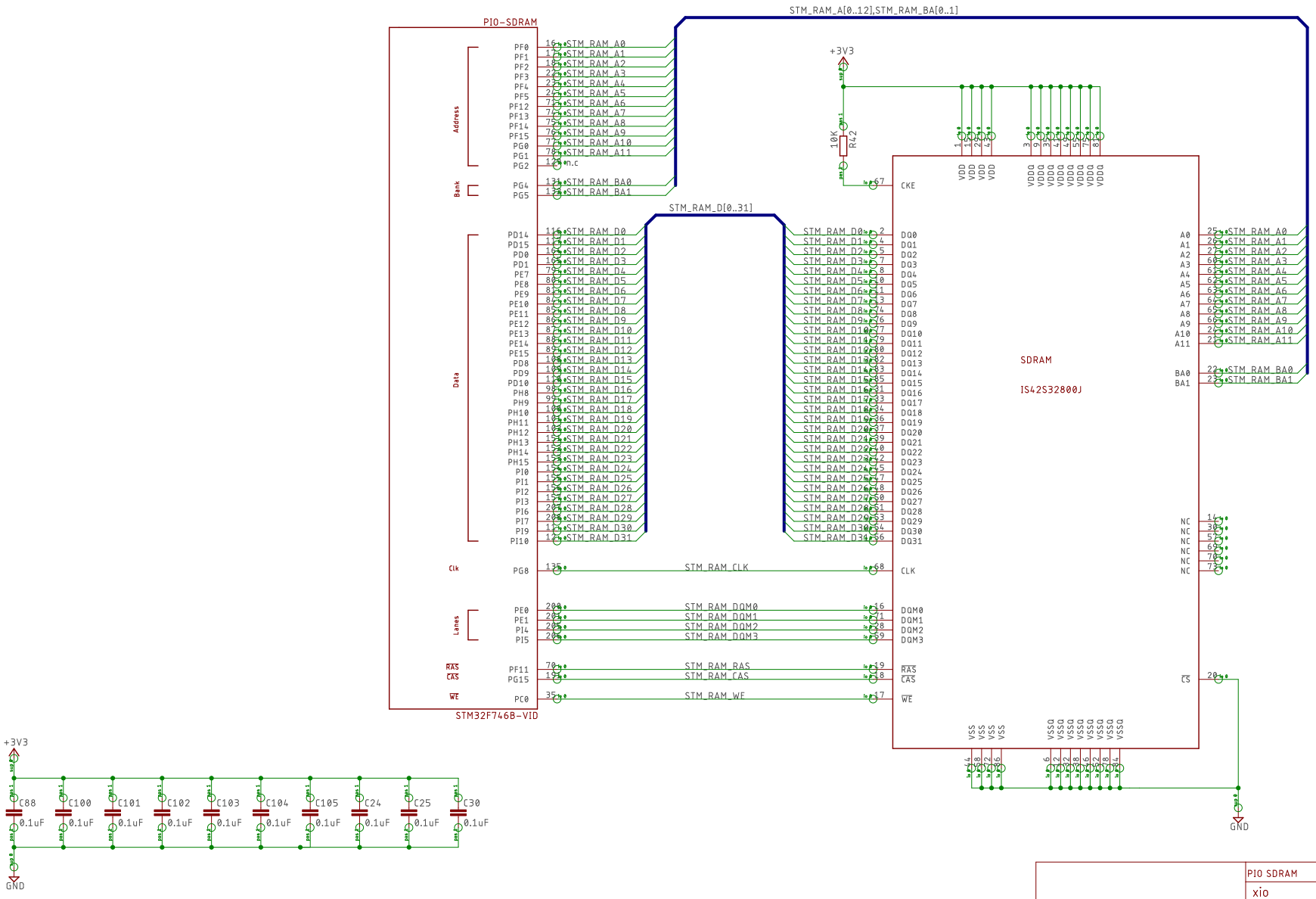
PIO-SDRAM
STM_RAM_A[0..12],STM_RAM_BA[0..1]
STM_RAM_D[0..31]
Address
Bank
Data
Clk
Lanes
RAS
CAS
WE
STM_RAM_A0
STM_RAM_A1
STM_RAM_A2
STM_RAM_A3
STM_RAM_A4
STM_RAM_A5
STM_RAM_A6
STM_RAM_A7
STM_RAM_A8
STM_RAM_A9
STM_RAM_A10
STM_RAM_A11
STM_RAM_BA0
STM_RAM_BA1
STM_RAM_CLK
STM_RAM_DQM0
STM_RAM_DQM1
STM_RAM_DQM2
STM_RAM_DQM3
STM_RAM_RAS
STM_RAM_CAS
STM_RAM_WE
+3V3
10K
R42
CKE
SDRAM
IS42S32800J
CLK
DQM0
DQM1
DQM2
DQM3
RAS
CAS
WE
CS
VDD
VDDQ
VSS
VSSQ
NC
STM32F746B-VID
C88
C100
C101
C102
C103
C104
C105
C24
C25
C30
0.1uF
GND
PIO SDRAM
xio
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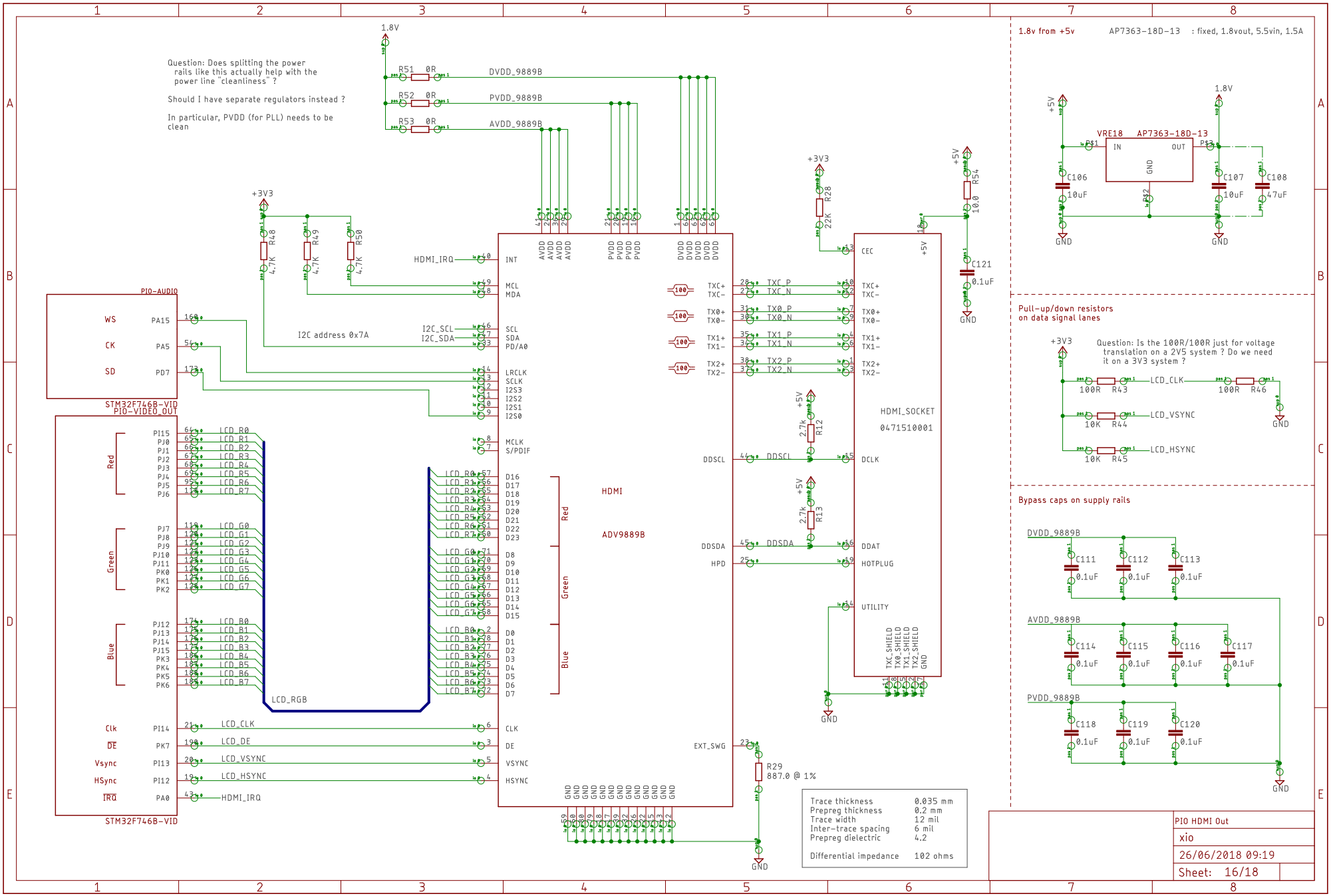
Question: Does splitting the power rails like this actually help with the power line "cleanliness" ?
Should I have separate regulators instead ?
In particular, PVDD (for PLL) needs to be clean
1.8V
R51 0R
R52 0R
R53 0R
DVDD_9889B
PVDD_9889B
AVDD_9889B
+3V3
R48 4.7K
R49 4.7K
R50 4.7K
I2C address 0x7A
HDMI_IRQ
I2C_SCL
I2C_SDA
INT
MCL
MDA
SCL
SDA
PD/A0
LRCLK
SCLK
I2S3
I2S2
I2S1
I2S0
MCLK
S/PDIF
AVDD
PVDD
DVDD
PIO-AUDIO
WS
CK
SD
PA15
PA5
PD7
STM32F746B-VID
PIO-VIDEO_OUT
Red
Green
Blue
LCD_R0
LCD_R1
LCD_R2
LCD_R3
LCD_R4
LCD_R5
LCD_R6
LCD_R7
LCD_G0
LCD_G1
LCD_G2
LCD_G3
LCD_G4
LCD_G5
LCD_G6
LCD_G7
LCD_B0
LCD_B1
LCD_B2
LCD_B3
LCD_B4
LCD_B5
LCD_B6
LCD_B7
LCD_RGB
D16
D17
D18
D19
D20
D21
D22
D23
D8
D9
D10
D11
D12
D13
D14
D15
D0
D1
D2
D3
D4
D5
D6
D7
HDMI
ADV9889B
Clk
DE
Vsync
HSync
IRQ
PI14
PK7
PI13
PI12
PA0
LCD_CLK
LCD_DE
LCD_VSYNC
LCD_HSYNC
CLK
DE
VSYNC
HSYNC
TXC+
TXC-
TX0+
TX0-
TX1+
TX1-
TX2+
TX2-
TXC_P
TXC_N
TX0_P
TX0_N
TX1_P
TX1_N
TX2_P
TX2_N
CEC
DDSCL
DDSDA
HPD
EXT_SWG
DDAT
HOTPLUG
UTILITY
DCLK
TXC.SHIELD
TX0.SHIELD
TX1.SHIELD
TX2.SHIELD
GND
HDMI_SOCKET
0471510001
R28 22K
R54 10.0
C121 0.1uF
R12 2.7k
R13 2.7k
R29 887.0 @ 1%
Trace thickness 0.035 mm
Prepreg thickness 0.2 mm
Trace width 12 mil
Inter-trace spacing 6 mil
Prepreg dielectric 4.2
Differential impedance 102 ohms
1.8v from +5v
AP7363-18D-13 : fixed, 1.8vout, 5.5vin, 1.5A
VRE18 AP7363-18D-13
IN
OUT
C106 10uF
C107 10uF
C108 47uF
R42
Pull-up/down resistors on data signal lanes
Question: Is the 100R/100R just for voltage translation on a 2V5 system ? Do we need it on a 3V3 system ?
100R R43
100R R46
10K R44
10K R45
LCD_CLK
LCD_VSYNC
LCD_HSYNC
Bypass caps on supply rails
C111 0.1uF
C112 0.1uF
C113 0.1uF
C114 0.1uF
C115 0.1uF
C116 0.1uF
C117 0.1uF
C118 0.1uF
C119 0.1uF
C120 0.1uF
PIO HDMI Out
xio
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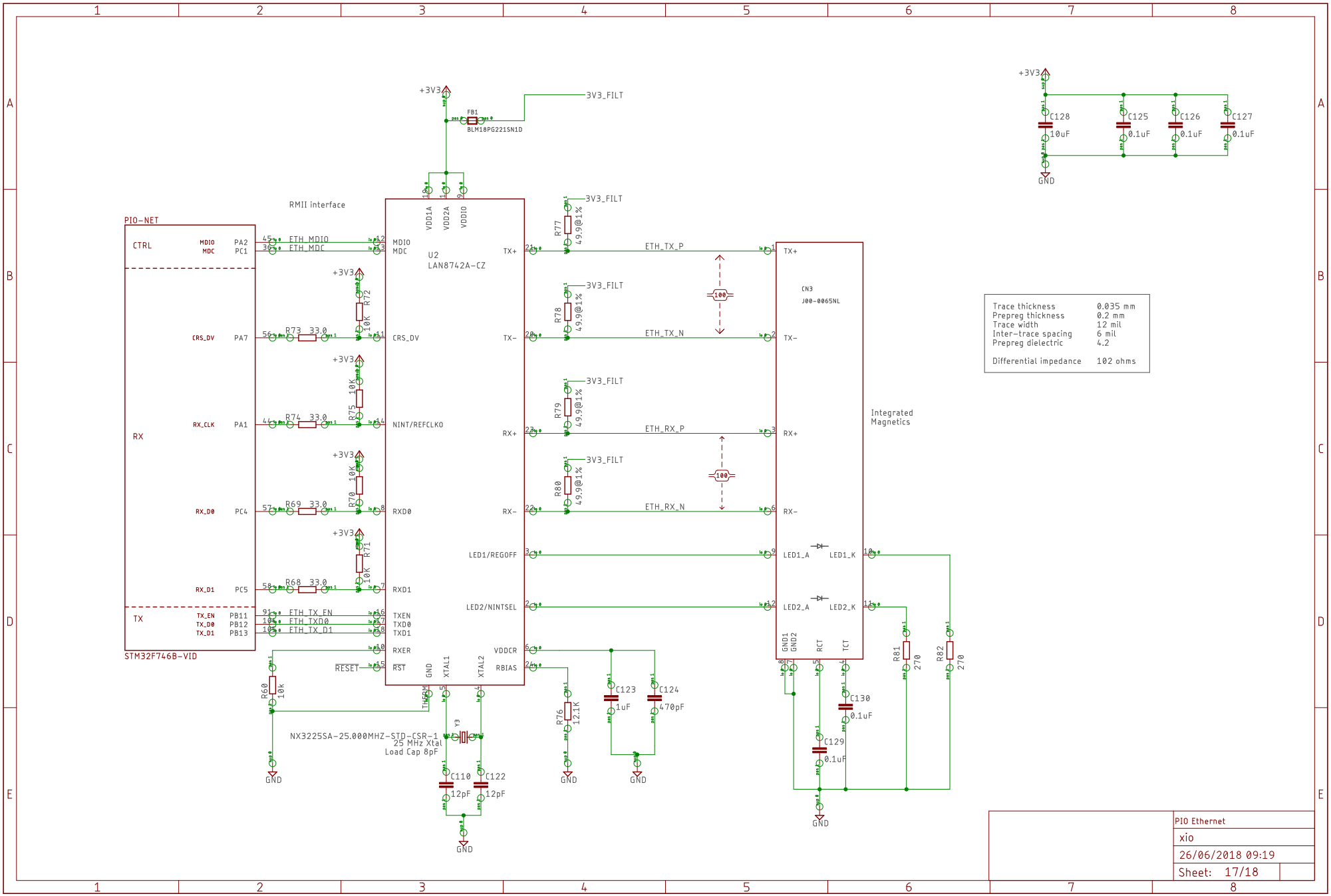
RMII interface
PIO-NET
CTRL
MDIO PA2
MDC PC1
RX
CRS_DV PA7
RX_CLK PA1
RX_D0 PC4
RX_D1 PC5
TX
TX_EN PB11
TX_D0 PB12
TX_D1 PB13
STM32F746B-VID
ETH_MDIO
ETH_MDC
ETH_TX_EN
ETH_TXD0
ETH_TX_D1
RESET
U2
LAN8742A-CZ
MDIO
MDC
CRS_DV
NINT/REFCLKO
RXD0
RXD1
TXEN
TXD0
TXD1
RXER
RST
VDD1A
VDD2A
VDDIO
GND
XTAL1
XTAL2
TXRM
VDDCR
RBIAS
LED1/REGOFF
LED2/NINTSEL
TX+
TX-
RX+
RX-
3V3_FILT
FB1
BLM18PG221SN1D
R72 10K
R73 33.0
R75 10K
R74 33.0
R70 10K
R69 33.0
R71 10K
R68 33.0
R60 10k
R77 49.9@1%
R78 49.9@1%
R79 49.9@1%
R80 49.9@1%
R76 12.1K
C123 1uF
C124 470pF
C110 12pF
C122 12pF
Y3
NX3225SA-25.000MHZ-STD-CSR-1
25 MHz Xtal
Load Cap 8pF
ETH_TX_P
ETH_TX_N
ETH_RX_P
ETH_RX_N
100
CN3
J00-0065NL
Integrated
Magnetics
LED1_A
LED1_K
LED2_A
LED2_K
GND1
GND2
RCT
TCT
R81 270
R82 270
C130 0.1uF
C129 0.1uF
C128 10uF
C125 0.1uF
C126 0.1uF
C127 0.1uF
Trace thickness 0.035 mm
Prepreg thickness 0.2 mm
Trace width 12 mil
Inter-trace spacing 6 mil
Prepreg dielectric 4.2
Differential impedance 102 ohms
PIO Ethernet
xio
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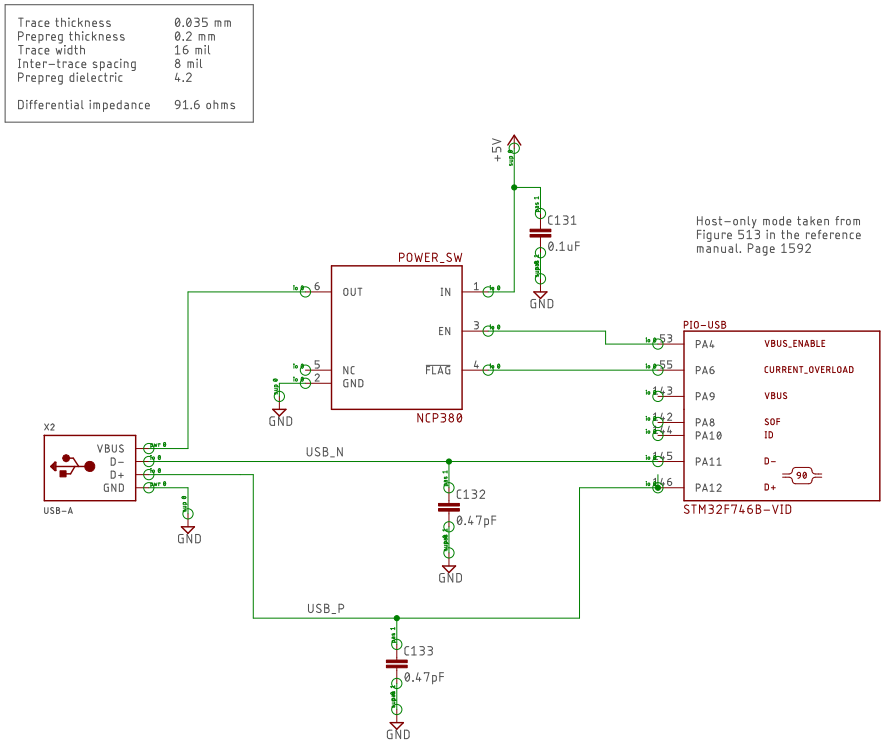

	PIO USB host-only mode
	xio
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